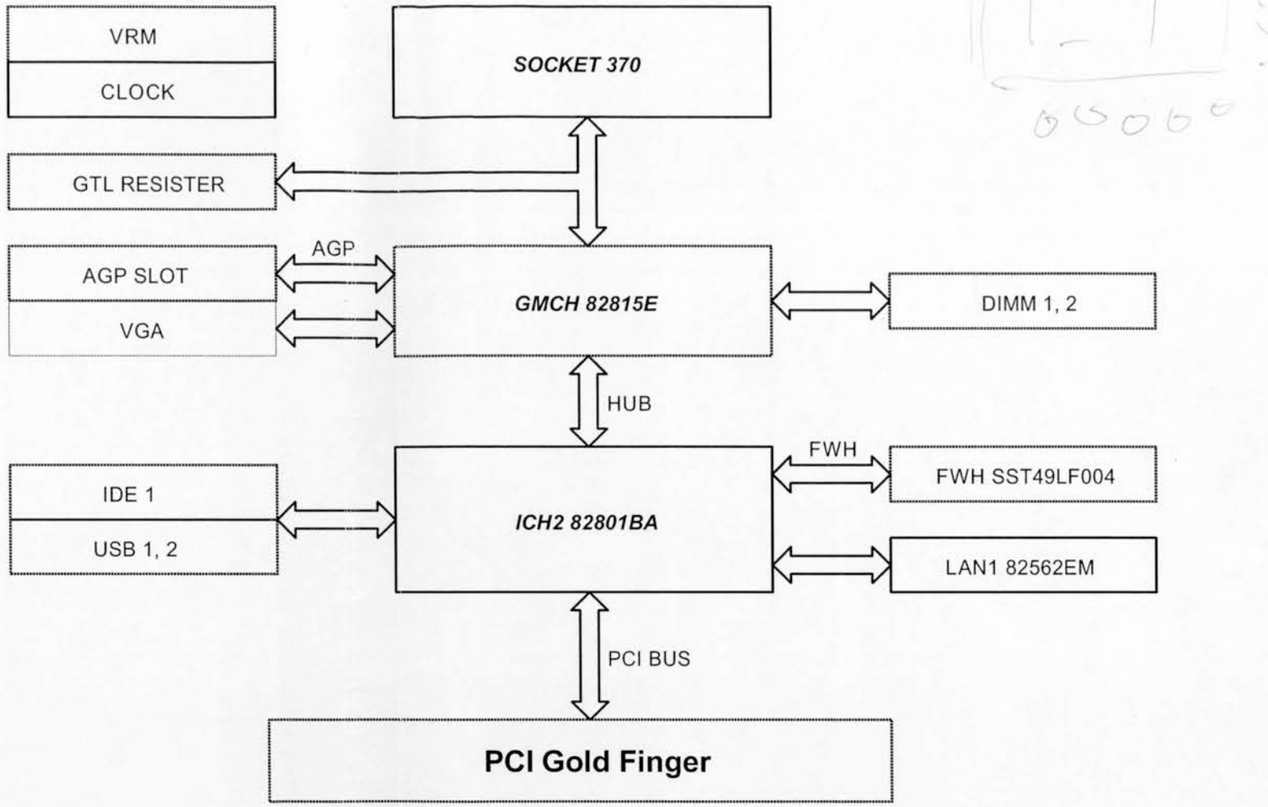
D815E

01	COVER SHEET
02	SOCKET370 1/2
03	SOCKET370 2/2
04	GTL RESISTER
05	CLOCK SYNTESIZER
06	GMCH_82815E 1/3
07	GMCH_82815E 2/3
08	GMCH_82815E 3/3
09	AGP SLOT
10	DIMM 1/2
11	DIMM 2/2
12	ICH2_82801BA 1/2
13	ICH2_82801BA 2/2
14	FWH
15	IDE CONNECTOR
16	USB PORT
17	PCI GF
18	VGA CONNECTOR
19	POWER
20	VRM_IRU3013
21	LAN1_82562EM

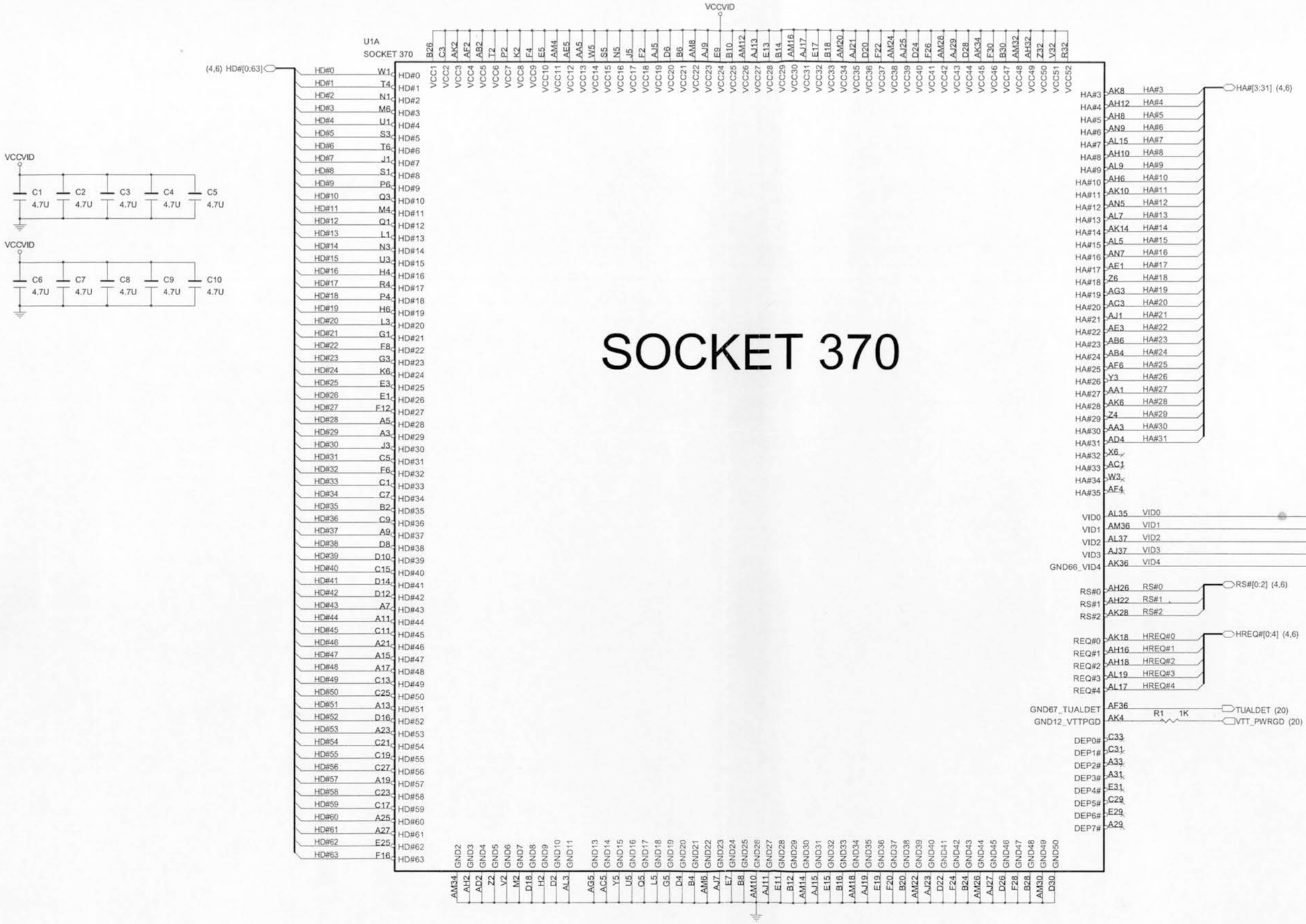


RTC- debe funcionar
BAT para la tension - VCMOS no ata en los esquemas
Posicionamiento de Socket 370
La señal VRM-PWRGD que sale del IRU3013 debe hacer la funcion de reset al bajar los 5Vcc por debajo de 4,70 Vcc ???
El modelo de conector no es AMP si no MOLEX (dos indicaron que no eran aceptados)
El conector del ventilador del pentium sera el standar de 3 pines CN9
Las distancias de socket 370 deben ser las standard para poner radiadores standard
En el Gold Finger que lado sera el de componets y cual el de soldaduras
La salida VGA sera de 8 pins 3 de masa y R, G, B, HSYNC, VSYNC en tres de pines.
La señal CLKG-VIDT porque esta conectada al diodo D1 del CLK Esquema 5

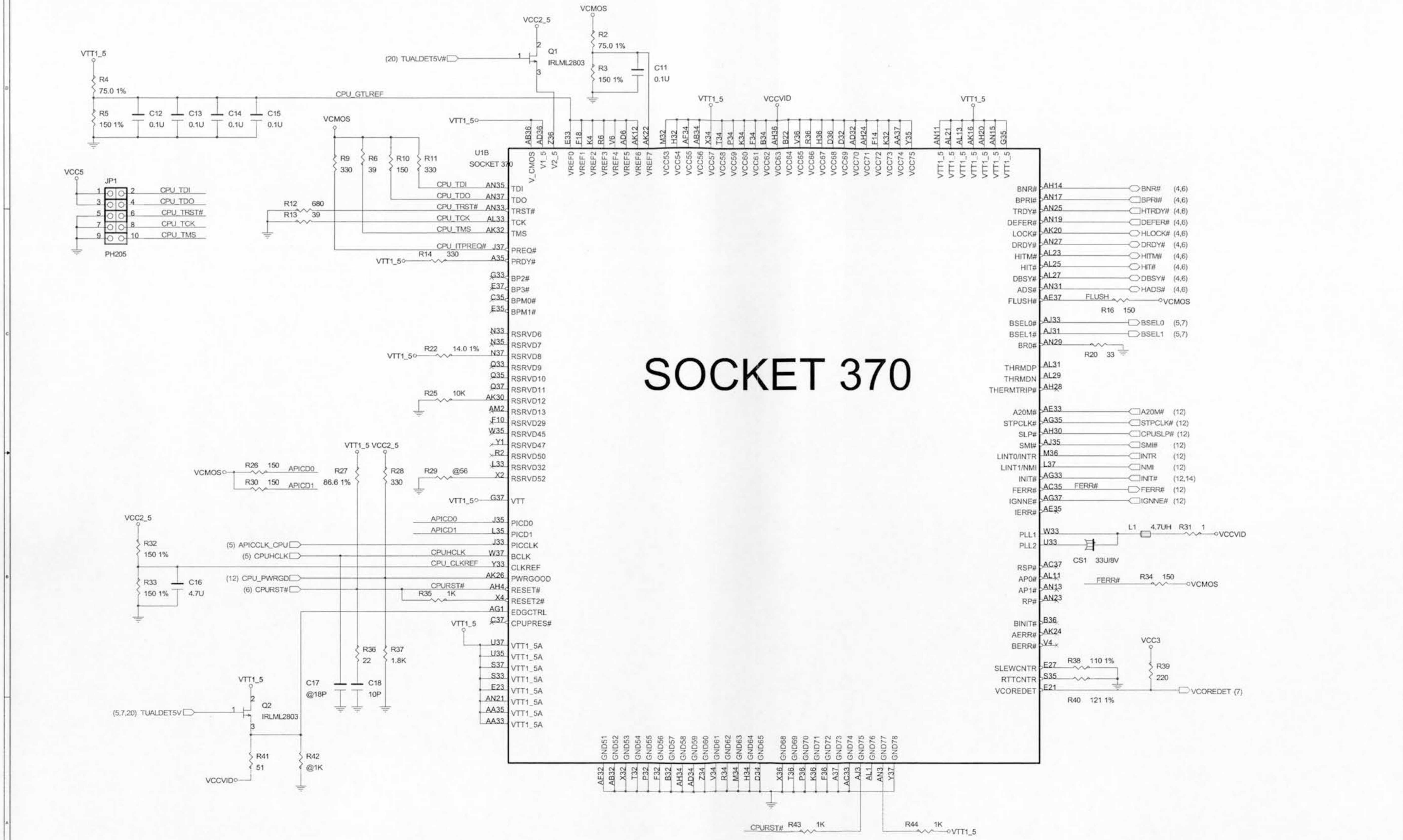
			EPoX COMPUTER CO., LTD		SCALE NONE	DRAWING DATE 2002-07-26	DRAWING TITLE D815E	Size A3	Description COVER SHEET	Rev. 0.0
			APPROVED MACRO	DESIGNED PING	DRAWN JOYCE	CUSTOMER NAME EPoX	JOB No. -	Sheet 1 of 21		

La 93C46-3.3V U11 del esquema 2.1 Es necesaria

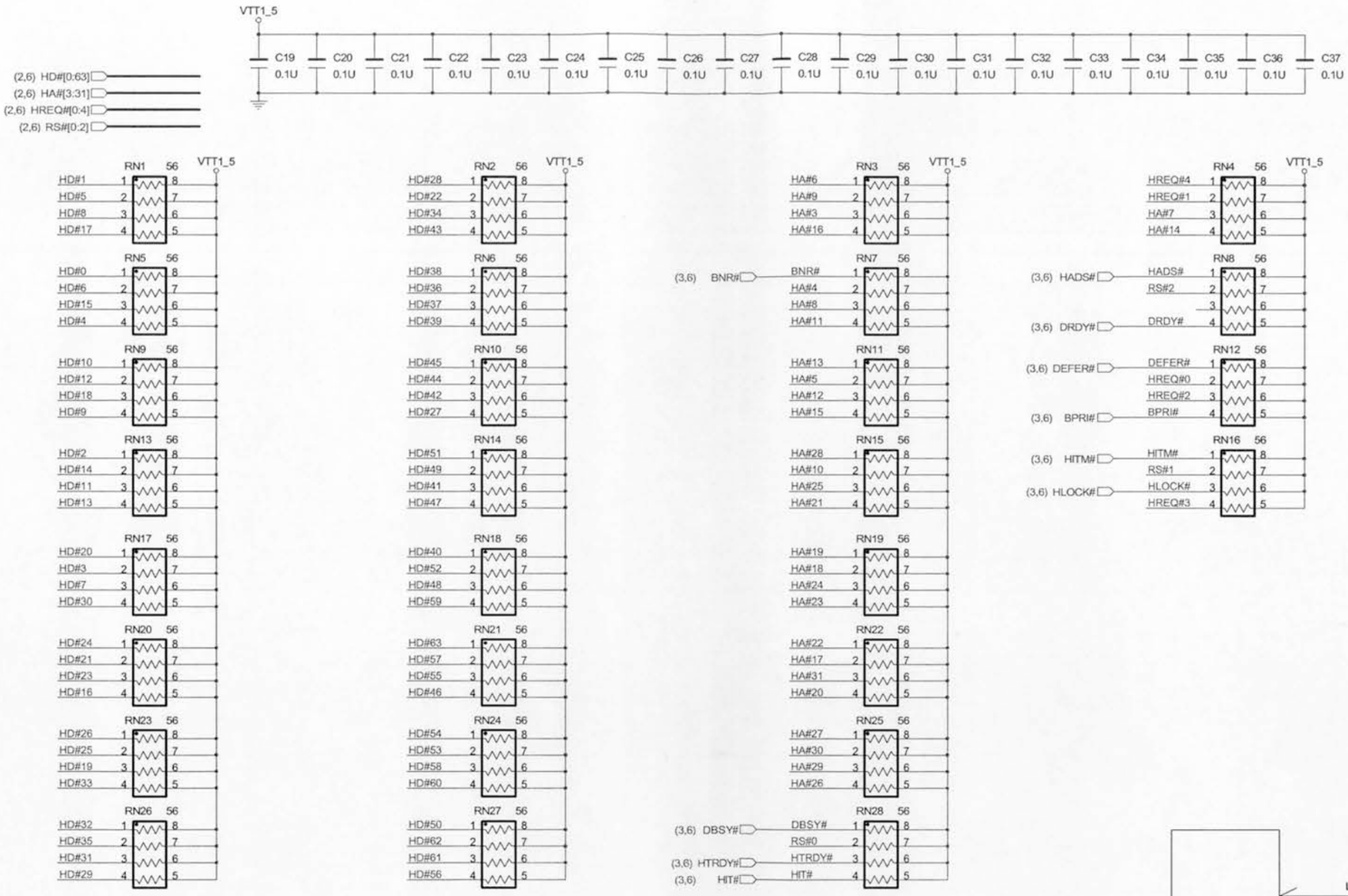
SOCKET 370



			EPoX COMPUTER CO., LTD	SCALE NONE	DRAWING DATE 2002-07-26	DRAWING TITLE D815E	Size A3	Description SOCKET370 1/2	Rev. 0.0
			APPROVED MACRO	DESIGNED PING	DRAWN JOYCE	CUSTOMER NAME EPoX	JOB No. -	Sheet 2 of 21	



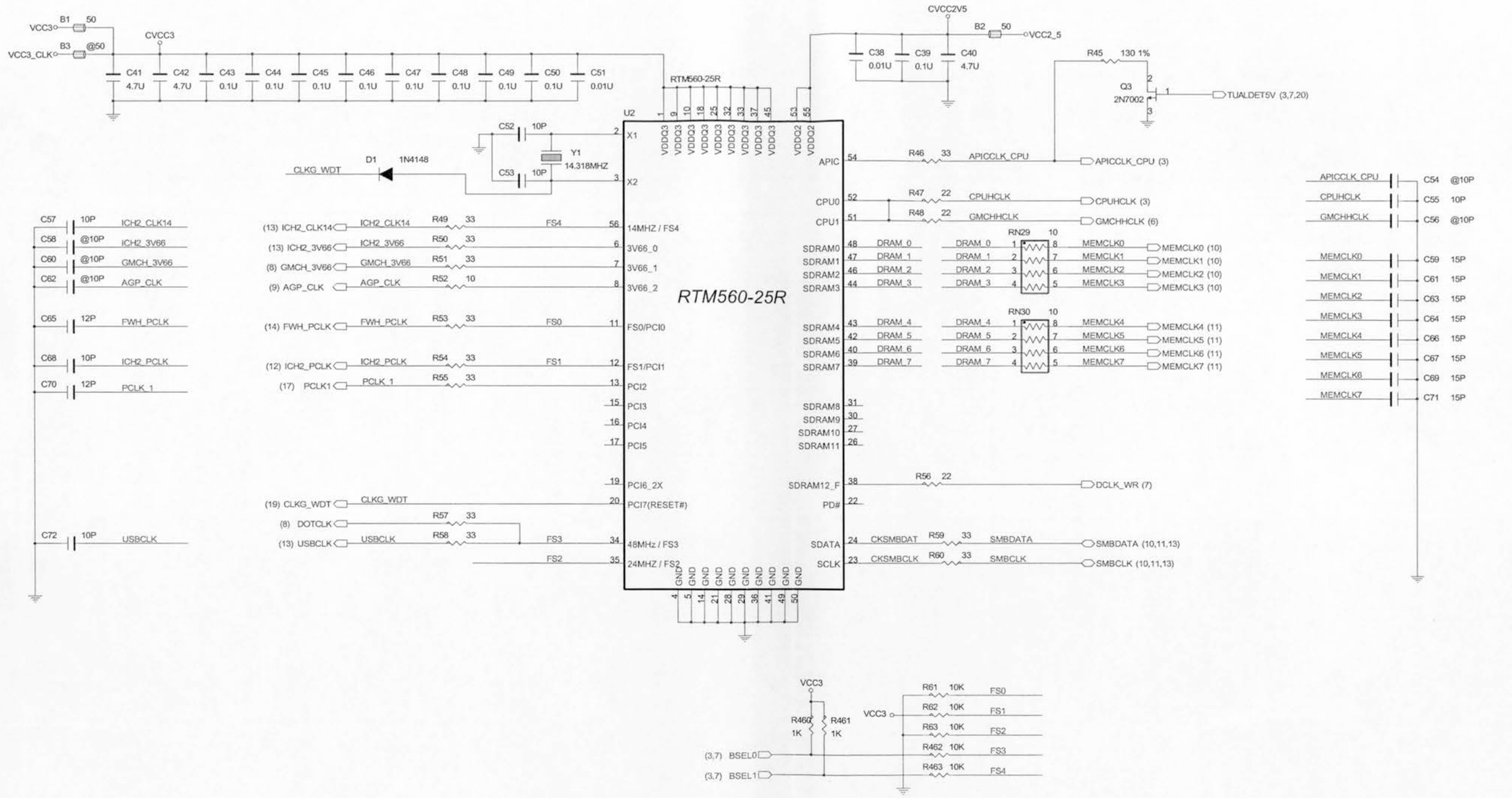
EPoX COMPUTER CO., LTD			SCALE NONE	DRAWING DATE 2002-07-26	DRAWING TITLE D815E	Size A3	Description SOCKET370 2/2	Rev. 0.0
APPROVED MACRO	DESIGNED PING	DRAWN JOYCE	CUSTOMER NAME EPoX		JOB No. -	Sheet 3	of 21	



	Min.(inch)	Max.(inch)
L1	1.90	4.50
L2	0	0
L3	0.50	2.50

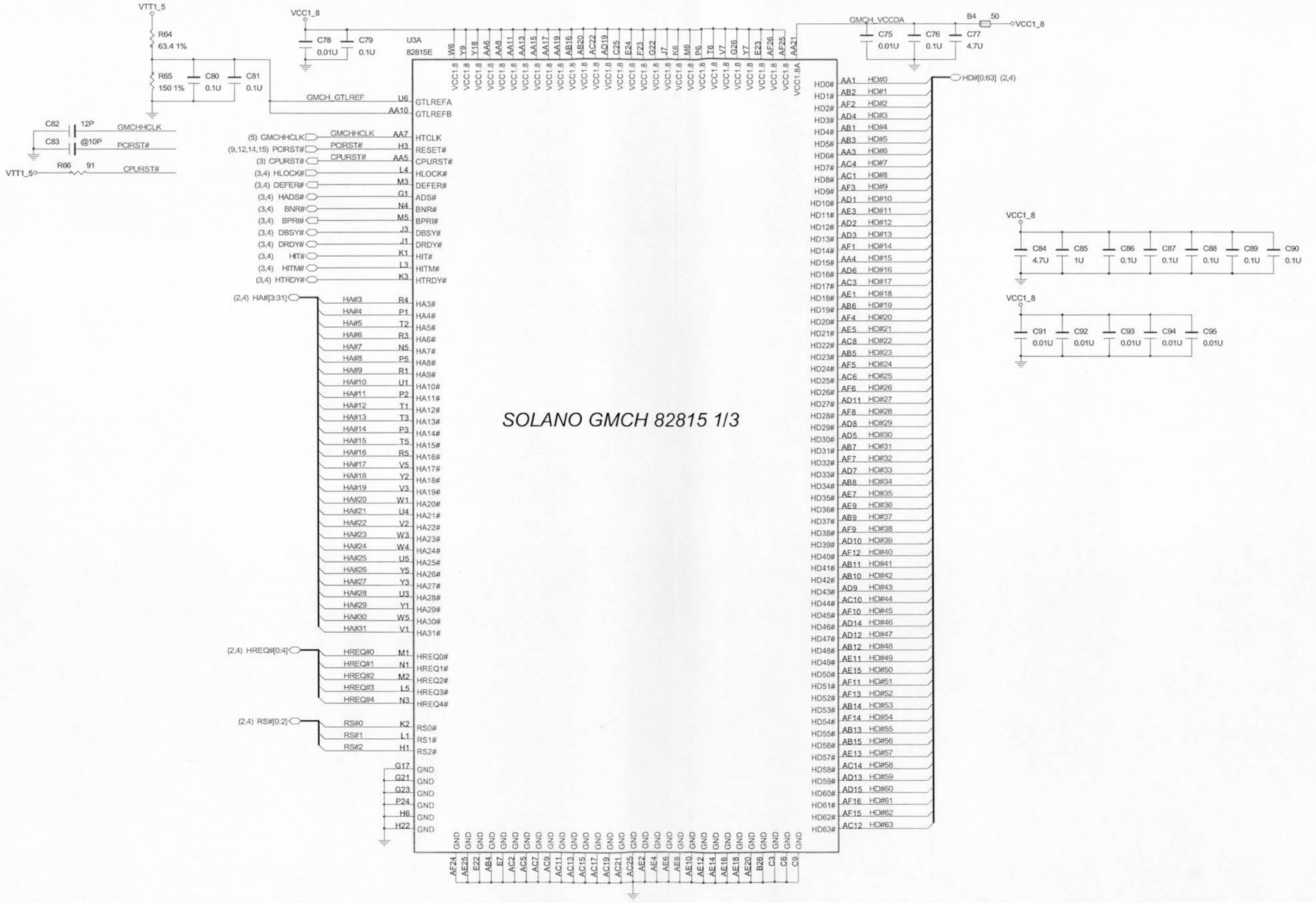
	Trace Width : Space Ratio (mil)
GTL Same group	5:10
GTL Different group	5:15
GTL to DIMM Group	5:30
GTL to non-GTL	5:20

			EPoX COMPUTER CO., LTD	SCALE NONE	DRAWING DATE 2002-07-26	DRAWING TITLE D815E	Size A3	Description GTL RESISTER	Rev. 0.0
			APPROVED MACRO	DESIGNED PING	DRAWN JOYCE	CUSTOMER NAME EPoX	JOB No. -	Sheet 4 of 21	



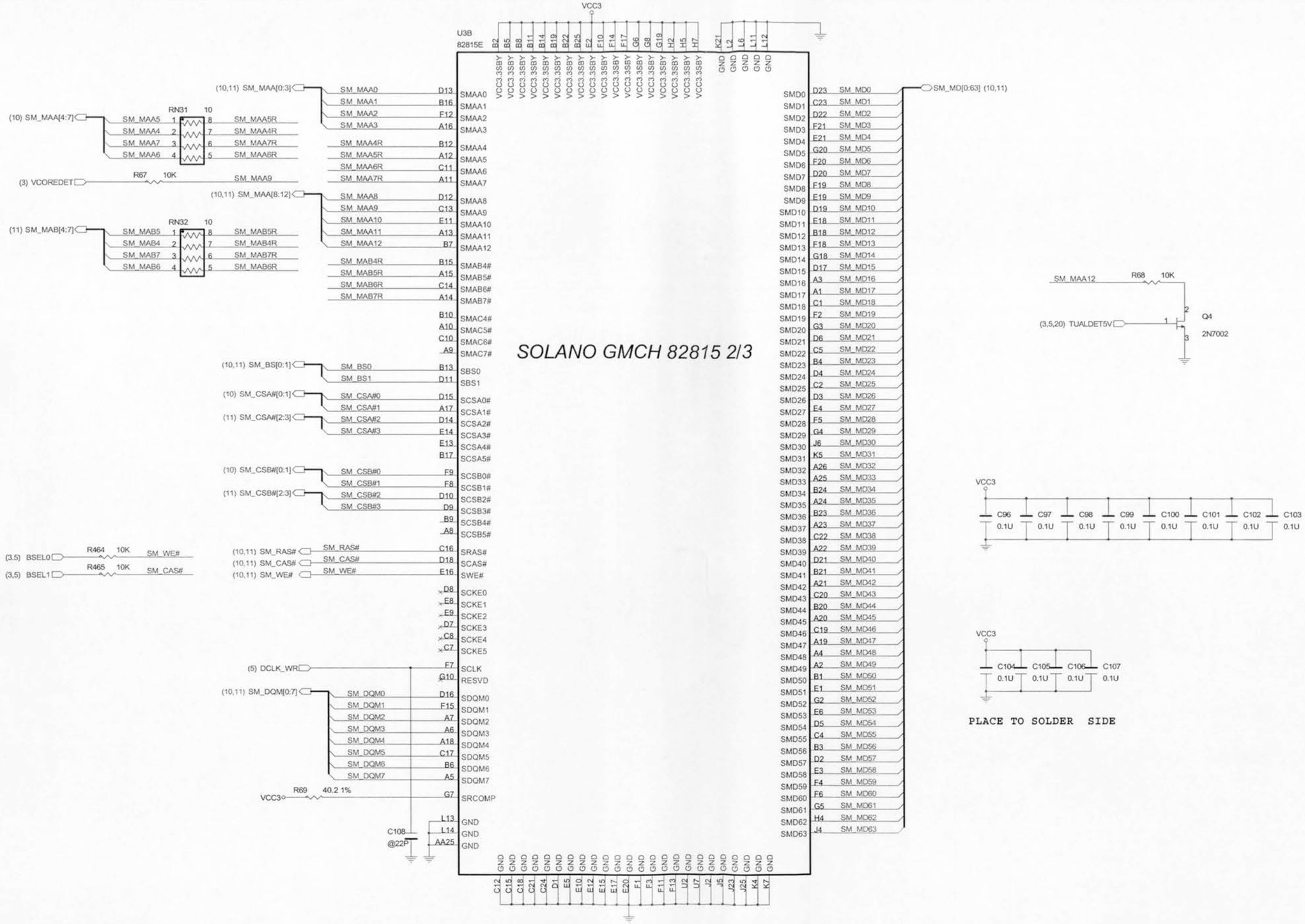
RTM560-25R

			EPoX COMPUTER CO., LTD		SCALE	DRAWING DATE	DRAWING TITLE	Size	Description / Rev.
					NONE	2002-07-26	D815E	A3	CLOCK SYNTESIZER / 0.0
			APPROVED	DESIGNED	DRAWN	CUSTOMER NAME	JOB No.	Sheet	5 of 21
			MACRO	PING	JOYCE	EPoX	-		



SOLANO GMCH 82815 1/3

			EPoX COMPUTER CO., LTD	SCALE	DRAWING DATE	DRAWING TITLE	Size	Description	Rev.
				NONE	2002-07-26	D815E	A3	GMCH_82815E 1/3	0.0
			APPROVED	DESIGNED	DRAWN	CUSTOMER NAME	JOB No.	Sheet 6 of 21	
			MACRO	PING	JOYCE	EPoX	-		



			EPoX COMPUTER CO., LTD	SCALE	DRAWING DATE	DRAWING TITLE	Size	Description	Rev.
				NONE	2002-07-26	D815E	A3	GMCH_82815E 2/3	0.0
			APPROVED	DESIGNED	DRAWN	CUSTOMER NAME	JOB No.	Sheet 7 of 21	
			MACRO	PING	JOYCE	EPoX	-		

SOLANO GMCH 82815 3/3

U3C
82815E

VDDQ
R70 301 1%
R71 200 1%
(9,19) TYPEDET#
Q5 2N7002
CAPGREF

(9) GAD[0:31]
GAD0 K26 GAD0/LDQM0
GAD1 J22 GAD1/LMD4
GAD2 K25 GAD2/LMD7
GAD3 J21 GAD3/LMD3
GAD4 L24 GAD4/LMD6
GAD5 J20 GAD5/LMD2
GAD6 L26 GAD6/LMD5
GAD7 K23 GAD7/LMD1
GAD8 K22 GAD8/LMD0
GAD9 M25 GAD9/LMA4
GAD10 M24 GAD10/LDQM1
GAD11 M26 GAD11/LMA2
GAD12 M21 GAD12/LMD8
GAD13 N24 GAD13/LMA5
GAD14 N22 GAD14/LMD9
GAD15 N26 GAD15/LMA1
GAD16 T26 GAD16/LMA8
GAD17 T22 GAD17/LMD14
GAD18 U24 GAD18/LMA11
GAD19 T23 GAD19/LMD15
GAD20 U26 GAD20/LMA9
GAD21 T24 GAD21/LMD16
GAD22 V24 GAD22/LCS#
GAD23 U21 GAD23/LMD17
GAD24 V25 GAD24/LCKE
GAD25 V21 GAD25/LMD18
GAD26 V26 GAD26/LCAS#
GAD27 W21 GAD27/LMD19
GAD28 W24 GAD28/LTCK1
GAD29 W22 GAD29/LMD20
GAD30 W26 GAD30/LTCK0
GAD31 Y21 GAD31/LMD21

(9) GCBE#[0:3]
GCBE#0 H23 GCBE#0/LMA3
GCBE#1 N21 GCBE#1/LMD11
GCBE#2 T25 GCBE#2/LMD13
GCBE#3 Y26 GCBE#3/LRAS#

(9) GFRAME# GFRAME# R26 GFRAME#/LMA10
(9) GDEVSEL# GDEVSEL# P26 GDEVSEL#/LMD11
(9) GIRDY# GIRDY# P23 GIRDY#/LMD12
(9) GTRDY# GTRDY# P21 GTRDY#/LMA7
(9) GSTOP# GSTOP# P25 GSTOP#/LMA0
(9) GPAR GPAR# R24 GPAR#/LMA6
(9) GREQ# GREQ# AE26 GREQ#/LMD27
(9) GGNT# GGNT# AD25 GGNT#
(9) PIPE# PIPE# AC26 PIPE#/LMD24

(9) ADSTB0 ADSTB0 M22 ADSTB0
(9) ADSTB0# ADSTB0# L23 ADSTB0#
(9) ADSTB1 ADSTB1 U22 ADSTB1
(9) ADSTB1# ADSTB1# V23 ADSTB1#
(9) SBSTB SBSTB Y23 SBSTB
(9) SBSTB# SBSTB# AA24 SBSTB#

(9) ST[0:2]
ST0 AD24 ST0/LMD28
ST1 AC24 ST1/LDQM3
ST2 AC23 ST2/LMD29

(9) RBF# RBF# AD26 RBF#/LMD30
(9) WBF# WBF# AB24 WBF#

(9) CAGPREF CAPGREF J24 AGPREF
R103 40.2 1% J26 GRCOMP
R104 10.0 1% OCLK R22 LOCLK
RCLK P22 LRCLK
R105 @8.2K
C124 22P

K20 K24 GND
Y24 V4 GND
L21 V6 GND
M23 Y20 GND
U25 V22 GND
N25 W2 GND
R21 W7 GND
U20 W23 GND
U23 W25 GND
W20 Y4 GND
Y6 GND
Y8 GND
Y10 GND
Y17 GND
Y19 GND
AA2 GND
AA9 GND
AA12 GND
AA14 GND
AA16 GND
P11 GND
P12 GND
P13 GND
P14 GND
P15 GND
VDDQ

LTVDATA0 AD16
LTVDATA1 AE17
LTVDATA2 AE17
LTVDATA3 AD17
LTVDATA4 AE18
LTVDATA5 AD18
LTVDATA6 AF20
LTVDATA7 AD20
LTVDATA8 AC20
LTVDATA9 AF21
LTVDATA10 AE21
LTVDATA11 AD21
LTVBLANK# AB19
TVCLKIN/SL_STALL AC18 R72 8.2K VCC3
LTVCLKOUT0 AE19
LTVCLKOUT1 AF19
TVVSYNC AC16
TVHSYNC AB17
LTVDA AB21 R75 8.2K VCC3
LTVCL AA20 R76 8.2K VCC3
R73 @8.2K R74 @8.2K
DDCCK AB18 R77 0 VGA_DDCCL (18)
DDCDA AA18 R78 0 VGA_DDCDA (18)
DCLKREF AE24 R79 0 DOTCLK (5)
IWASTE Y20
IREF AD23 RSET R80 @8.2K
R81 174 1%
C119 18P
VSYNC AF22 R82 0 VGA_VSYNC (18)
HSYNC AF23 R83 0 VGA_HSYNC (18)
RED AD22 R84 0 VGA_RED (18)
GREEN AE22 R85 0 VGA_GREEN (18)
BLUE AE23 R86 0 VGA_BLUE (18)
HLCLK F22 GMCH_3V66 GMCH_3V66 (5)
HL0 H24 HL0
HL1 H26 HL1
HL2 H25 HL2
HL3 G24 HL3
HL4 F24 HL4
HL5 E26 HL5
HL6 E25 HL6
HL7 D26 HL7
HL8 D25 HL8
HL9 D24 HL9
HL10 C26 HL10 HL[0:10] (12)
HUBREF H21 GMCH_HUBREF
HLSTRB G25 HLSTB HLSTB (12)
HLSTRB# F26 HLSTB# HLSTB# (12)
HLZCOMP H20 R96 40.2 1% VCC1_8
SBA0/LMD31 AB22 SBA0
SBA1/LMD25 AB25 SBA1
SBA2/LDQM2 AB23 SBA2
SBA3/LMD26 AB26 SBA3
SBA4/LMD23 AA22 SBA4
SBA5/WE# AA26 SBA5
SBA6/LMD22 Y22 SBA6
SBA7/LGM_FREQ_SEL Y25 SBA7
SBA[0:7] (9)

GND N16 GND N23 GND P4 GND AA23 GND F16 GND F25 GND G9
GND P16 GND R2 GND R6 GND R11 GND R12 GND R13 GND R14 GND R15 GND R16 GND R23 GND R25 GND T4 GND T11 GND T12 GND T13 GND T14 GND T15 GND T16 GND L15 GND L16 GND L22 GND L25 GND M4 GND M11 GND M12 GND M13 GND M14 GND M15 GND M16 GND N2 GND N6 GND N11 GND N12 GND N13 GND N14 GND N15

VDDQ
C109 0.1U C110 0.1U C111 0.1U C112 0.1U C113 0.1U C114 0.1U C115 0.1U
VDDQ
C116 @0.1U C117 @0.1U C118 @0.1U

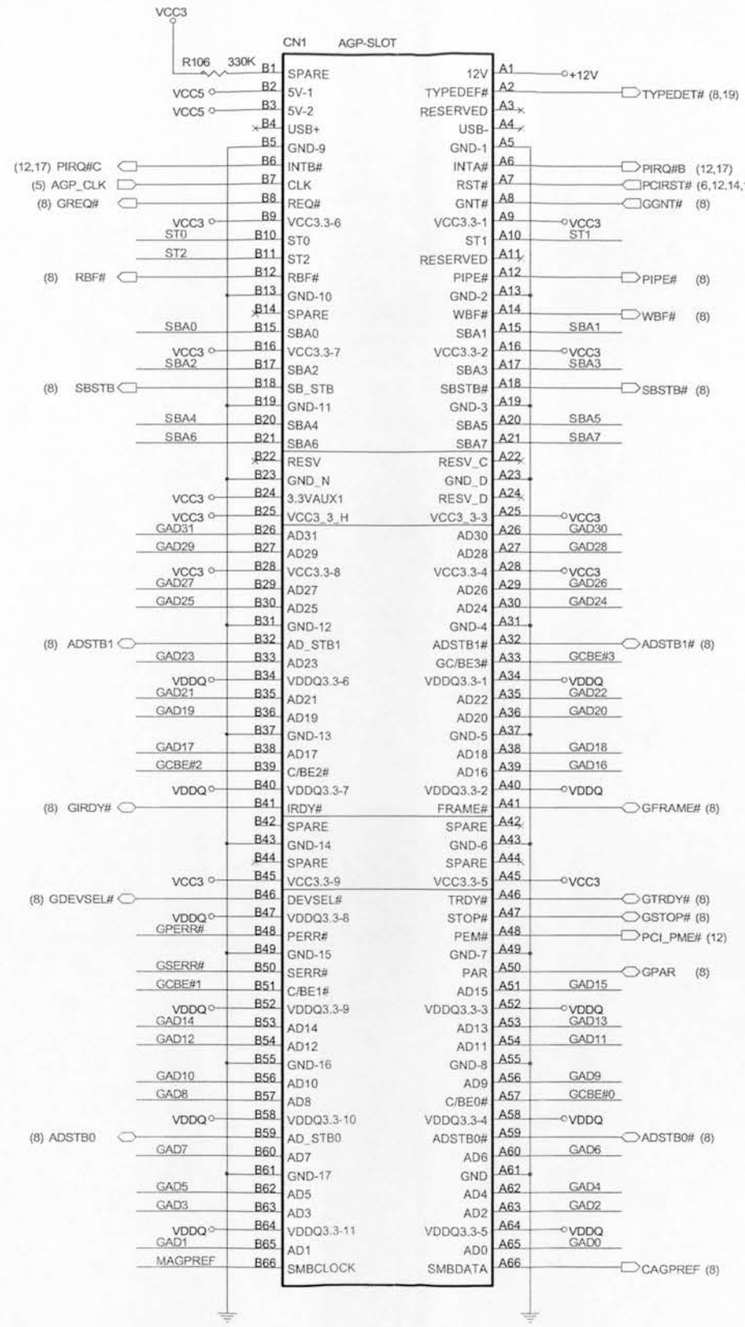
GMCH_3V66
C120 22P
VCC1_8
R87 301 1%
C121 0.01U C122 0.1U R90 301 1%

RN33 8.2K
4 5 GTRDY#
3 6 GDEVSEL#
2 7 GIRDY#
1 8 GFRAME#
RN34 8.2K
1 8 GGNT#
2 7 GREQ#
3 6 GSTOP#
4 5
R88 8.2K PIPE#
R89 8.2K RBF#
R91 8.2K ADSTB0
R92 8.2K ADSTB1
R93 8.2K WBF#
R94 8.2K SBSTB
R95 8.2K ST0
R97 8.2K ST1
R98 8.2K ST2
R99 8.2K GPAR#
R100 8.2K ADSTB0#
R101 8.2K ADSTB1#
R102 8.2K SBSTB#
VCC3
C123 0.1U CAPGREF

19+5
24

EPoX COMPUTER CO., LTD			SCALE: NONE	DRAWING DATE: 2002-07-26	DRAWING TITLE: D815E	Size: A3	Description: GMCH_82815E 3/3	Rev.: 0.0
APPROVED: MACRO	DESIGNED: PING	DRAWN: JOYCE	CUSTOMER NAME: EPoX		JOB No.: -	Sheet 8 of 21		

(8) GAD[0:31]
(8) GCBE#[0:3]
(8) ST[0:2]
(8) SBA[0:7]

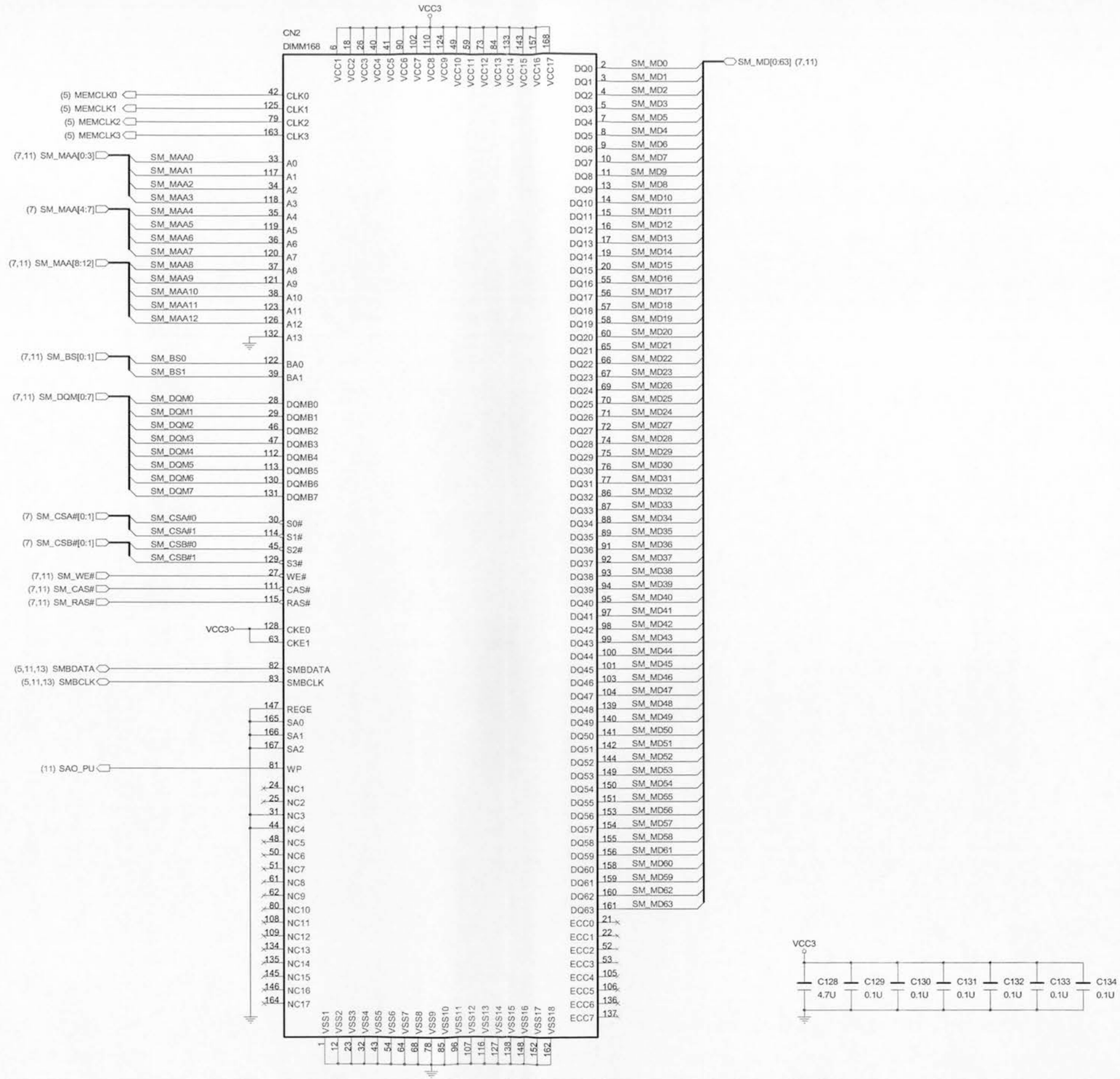


VDDQ
CE1 6MV1000CA
CE2 6MV1000CA

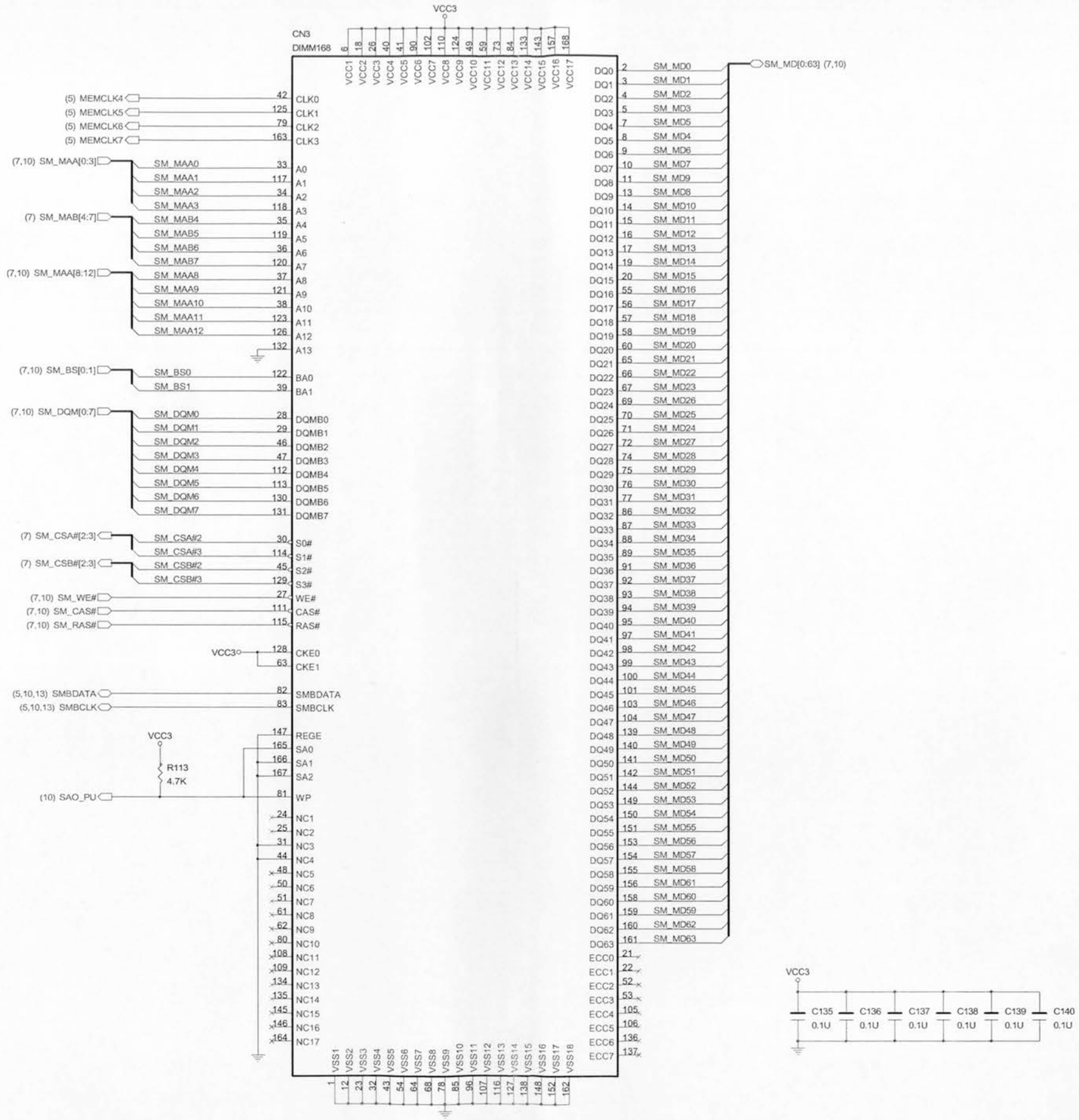
VCC3
R107 8.2K GPERR#
R108 8.2K GSERR#

VDDQ
C125 470P
R109 82
R110 1K
MAGPREF
R111 82
R112 1.5K
C126 0.1U
C127 470P

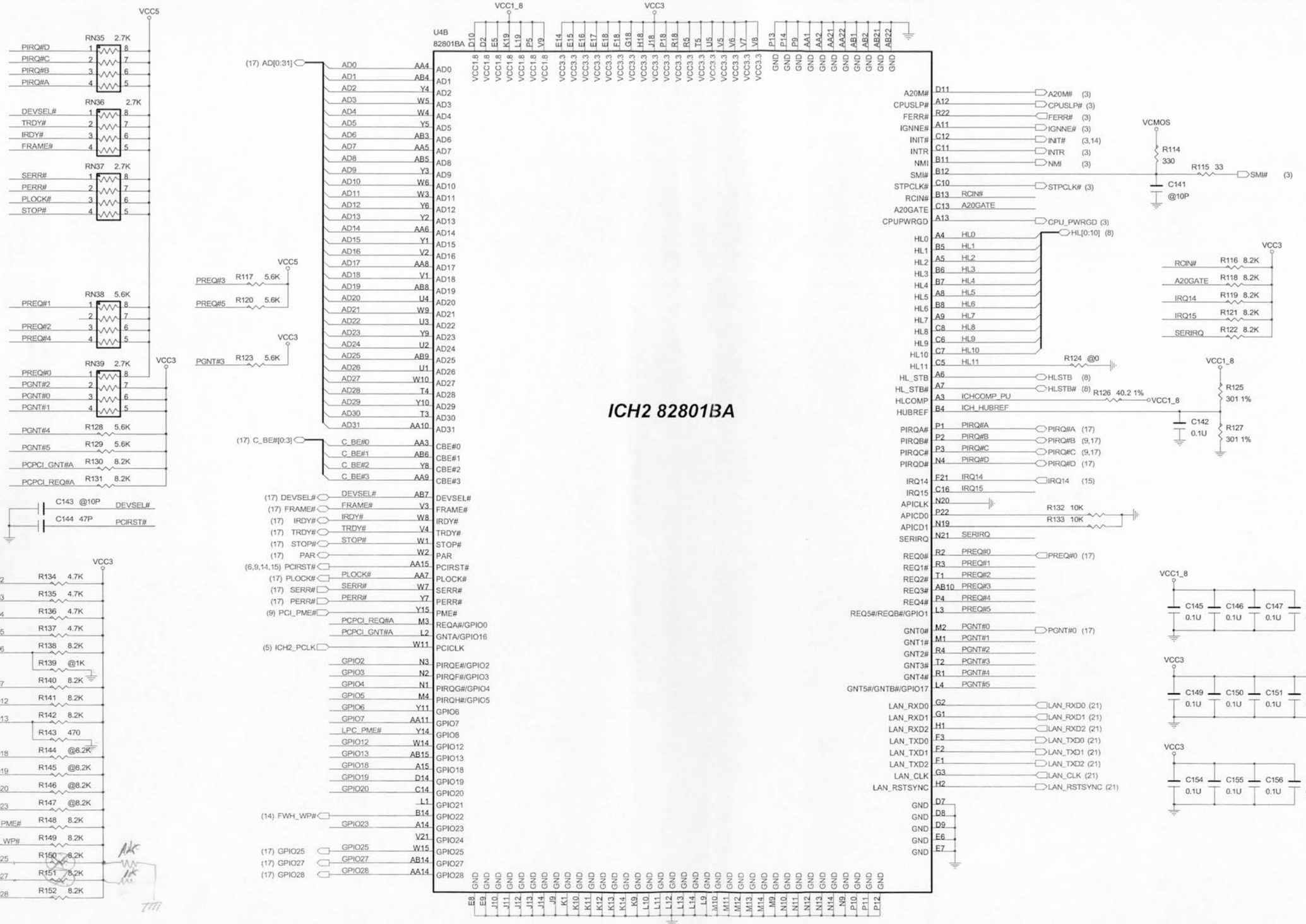
		EPoX COMPUTER CO., LTD		SCALE NONE	DRAWING DATE 2002-07-26	DRAWING TITLE D815E	Size A3	Description AGP SLOT	Rev. 0.0
		APPROVED MACRO	DESIGNED PING	DRAWN JOYCE	CUSTOMER NAME EPoX	JOB No. -	Sheet 9 of 21		



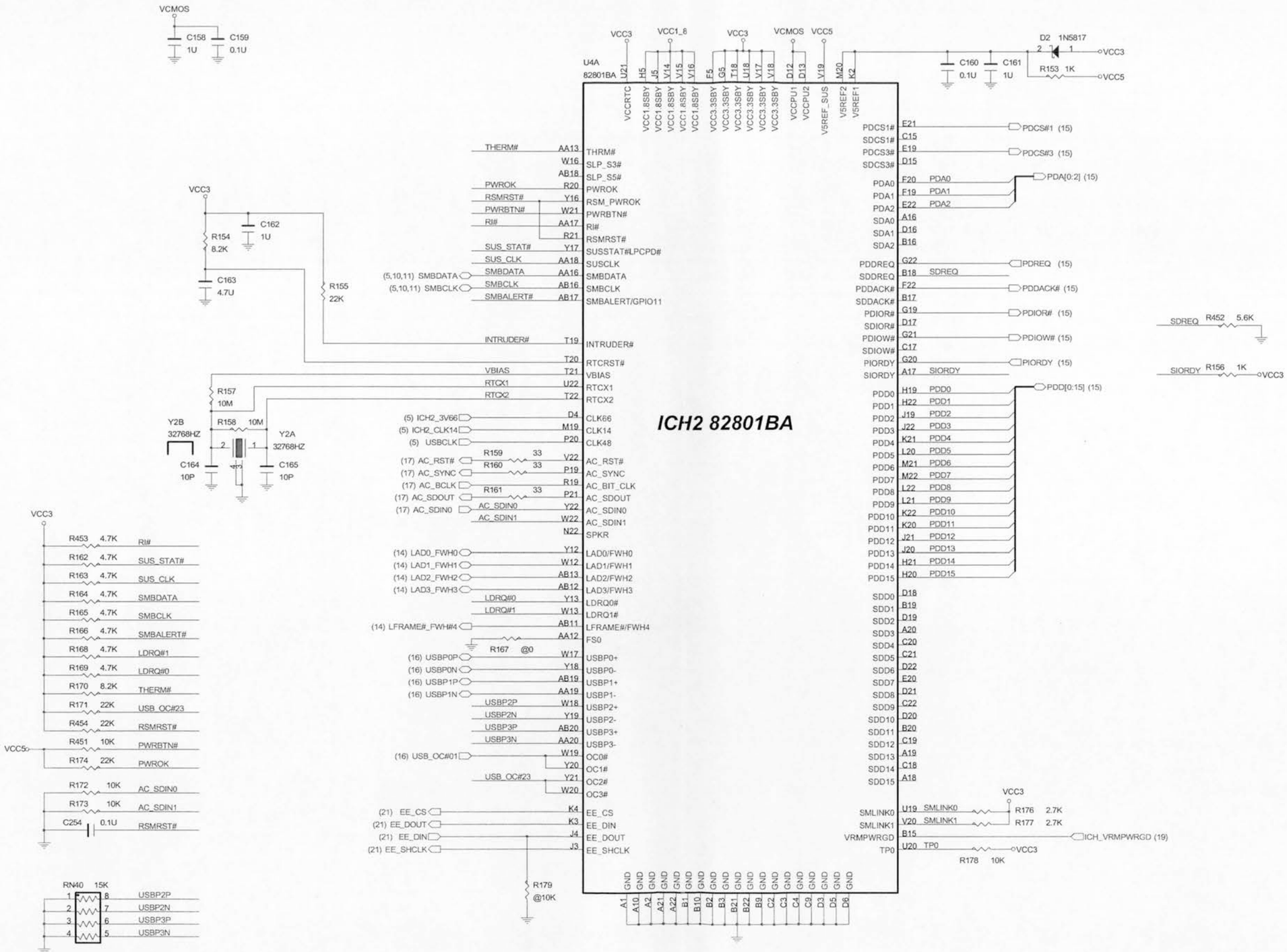
	EPoX COMPUTER CO., LTD		SCALE: NONE	DRAWING DATE: 2002-07-26	DRAWING TITLE: D815E	Size: A3	Description: DIMM 1/2	Rev.: 0.0
	APPROVED: MACRO	DESIGNED: PING	DRAWN: JOYCE	CUSTOMER NAME: EPoX	JOB No.: -	Sheet 10 of 21		



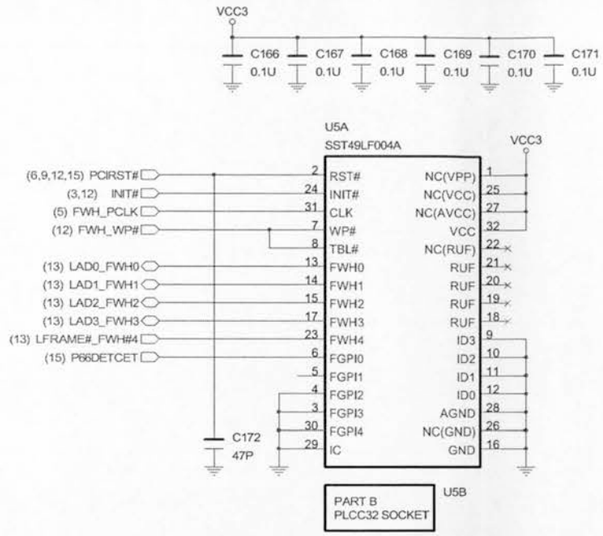
			EPoX COMPUTER CO., LTD	SCALE: NONE	DRAWING DATE: 2002-07-26	DRAWING TITLE: D815E	Size: A3	Description: DIMM 2/2	Rev.: 0.0
			APPROVED: MACRO	DESIGNED: PING	DRAWN: JOYCE	CUSTOMER NAME: EPoX	JOB No.: -	Sheet 11 of 21	



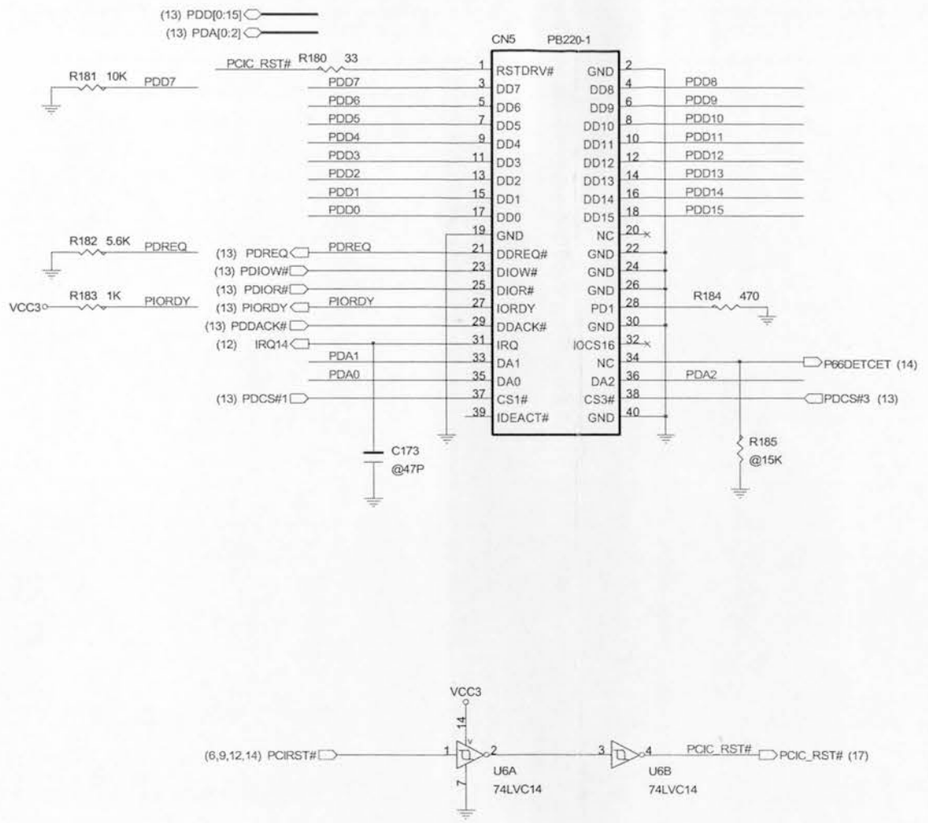
			EPoX COMPUTER CO., LTD		SCALE	DRAWING DATE	DRAWING TITLE	Size	Description / Rev.
					NONE	2002-07-26	D815E	A3	ICH2_82801BA 1/2 / 0.0
			APPROVED	DESIGNED	DRAWN	CUSTOMER NAME	JOB No.	Sheet	
			MACRO	PING	JOYCE	EPoX	-	12 of 21	



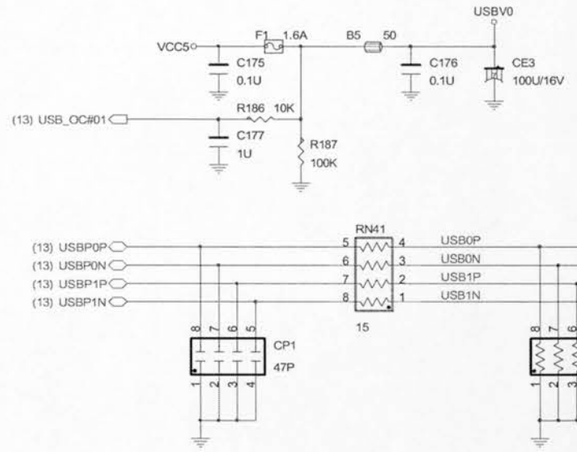
		EPoX COMPUTER CO., LTD			SCALE NONE	DRAWING DATE 2002-07-26	DRAWING TITLE D815E	Size A3	Description ICH2_82801BA 2/2	Rev. 0.0
		APPROVED MACRO	DESIGNED PING	DRAWN JOYCE	CUSTOMER NAME EPoX		JOB No. -	Sheet 13 of 21		



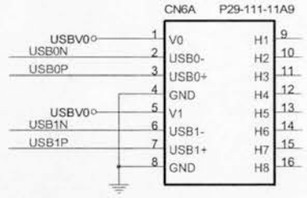
△			EPoX COMPUTER CO., LTD		SCALE: NONE	DRAWING DATE: 2002-07-26	DRAWING TITLE: D815E	Size: A3	Description: FWH_SST49LF004	Rev.: 0.0
△										
△			APPROVED: MACRO	DESIGNED: PING	DRAWN: JOYCE	CUSTOMER NAME: EPoX	JOB No.: -	Sheet 14 of 21		
△										



△			EPoX COMPUTER CO., LTD			SCALE NONE	DRAWING DATE 2002-07-26	DRAWING TITLE D815E	Size A3	Description IDE CONNECTOR	Rev. 0.0
△											
△			APPROVED MACRO	DESIGNED PING	DRAWN JOYCE	CUSTOMER NAME EPoX		JOB No. -	Sheet 15 of 21		
△											

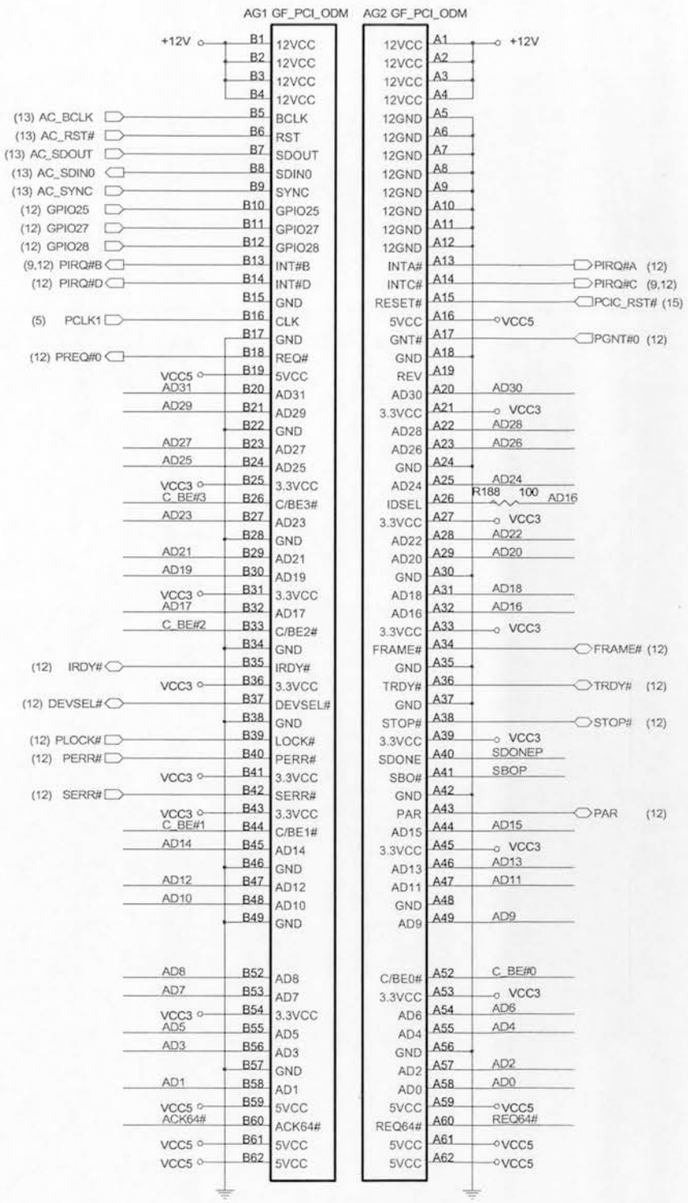


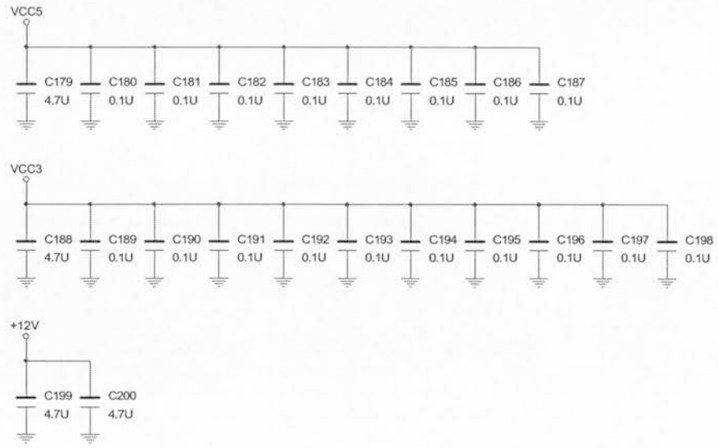
USB PORT

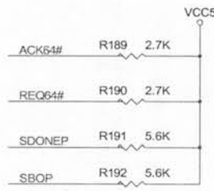


			EPoX COMPUTER CO., LTD		SCALE NONE	DRAWING DATE 2002-07-26	DRAWING TITLE D815E	Size A3	Description USB PORT	Rev. 0.0
			APPROVED MACRO	DESIGNED PING	DRAWN JOYCE	CUSTOMER NAME EPoX	JOB No. -	Sheet 16 of 21		

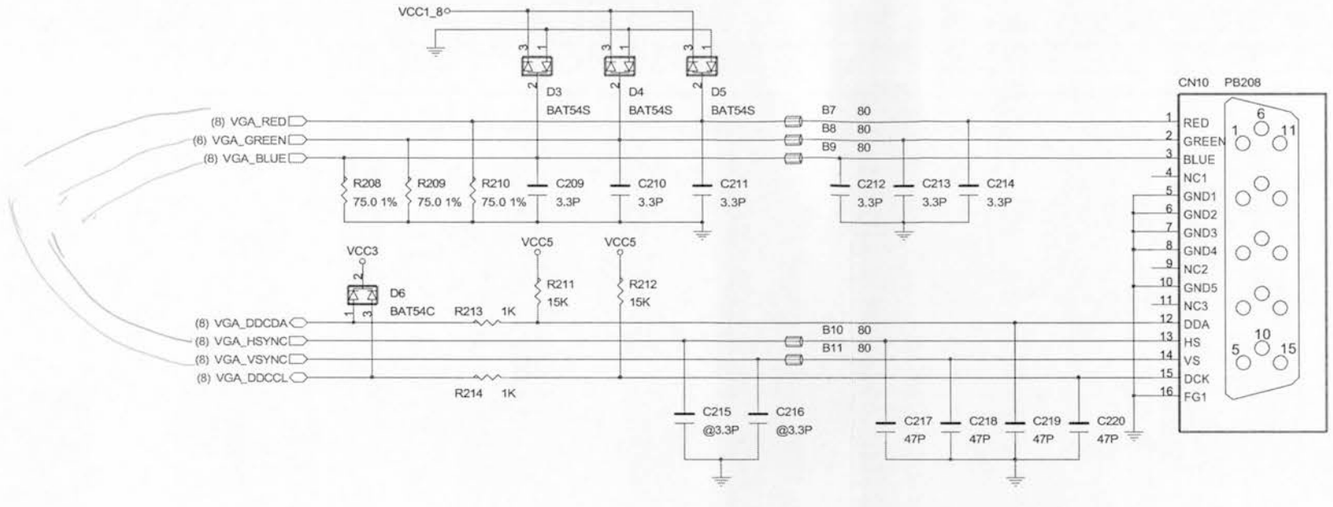
(12) AD[0:31]
(12) C_BE#[0:3]



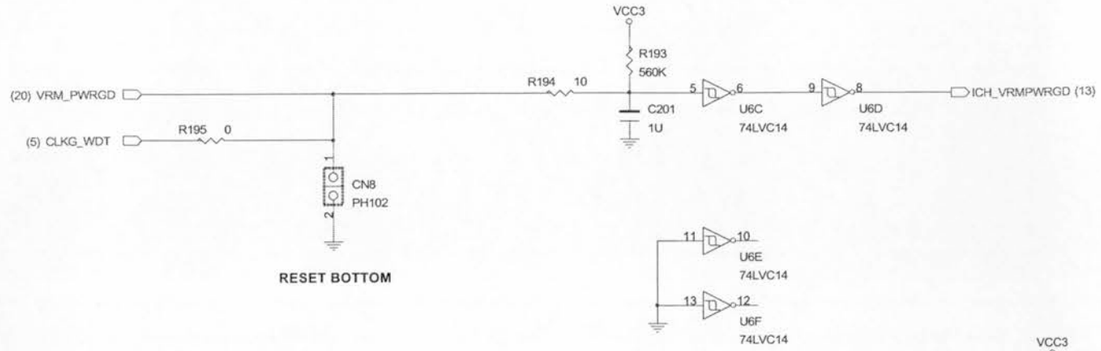


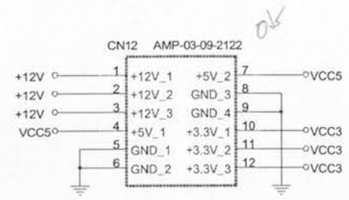


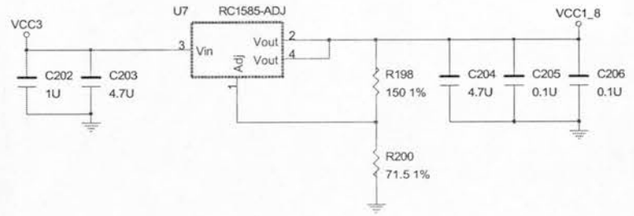
			EPoX COMPUTER CO., LTD		SCALE NONE	DRAWING DATE 2002-07-26	DRAWING TITLE D815E	Size A3	Description PCI GF	Rev. 0.0
			APPROVED MACRO	DESIGNED PING	DRAWN JOYCE	CUSTOMER NAME EPoX	JOB No. -	Sheet 17 of 21		

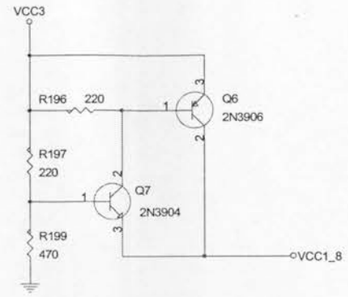


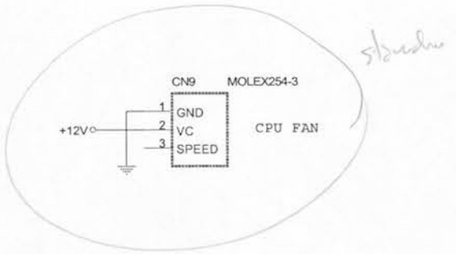
		EPoX COMPUTER CO., LTD		SCALE NONE	DRAWING DATE 2002-07-26	DRAWING TITLE D815E	Size A3	Description VGA CONNECTOR	Rev. 0.0
		APPROVED MACRO	DESIGNED PING	DRAWN JOYCE	CUSTOMER NAME EPoX	JOB No. -	Sheet 18 of 21		

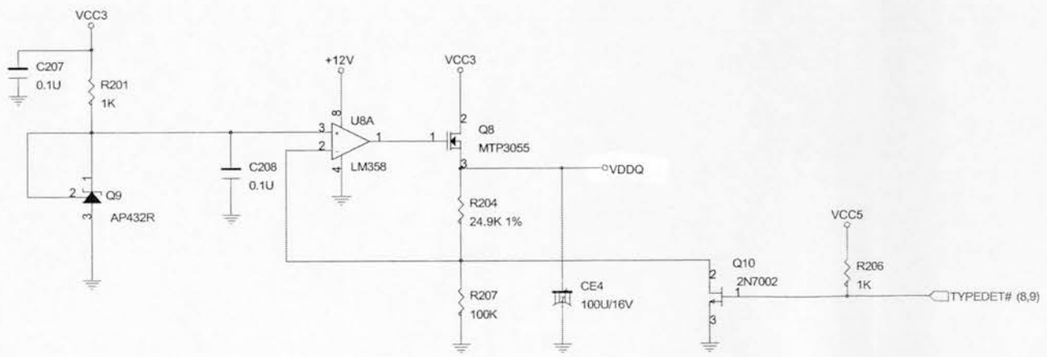


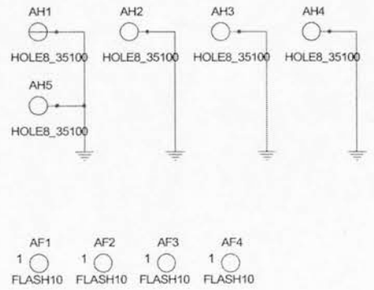




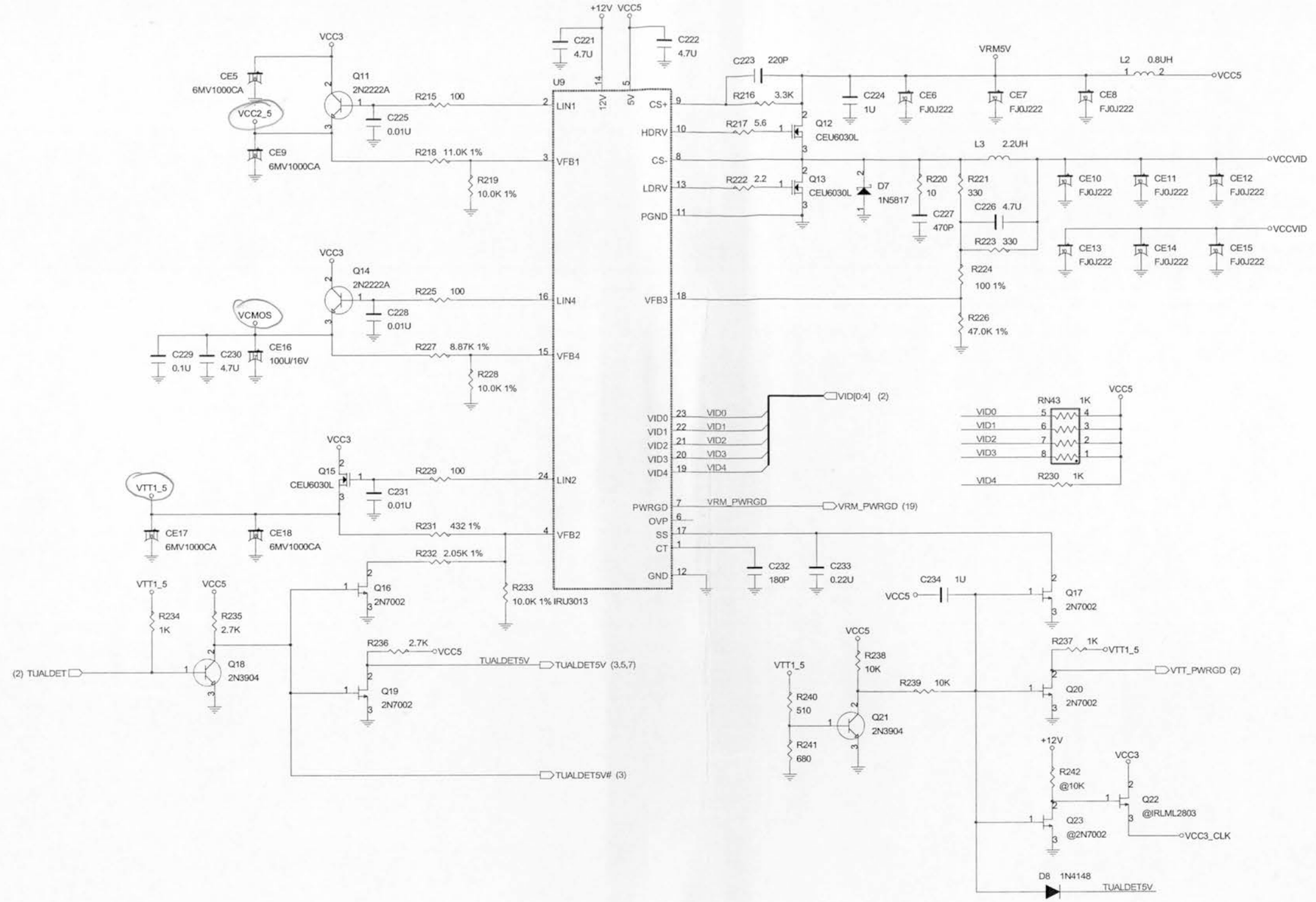




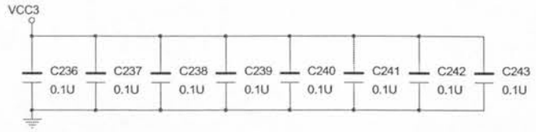


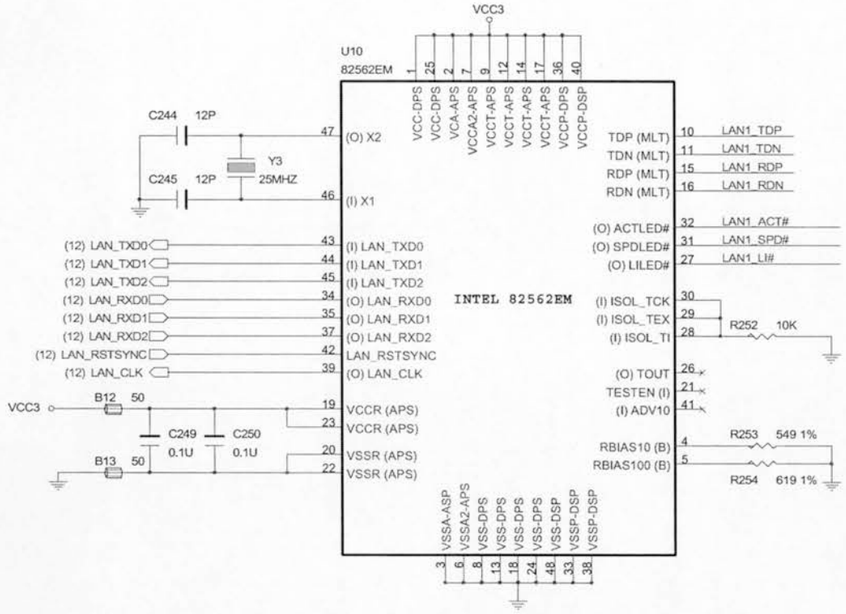


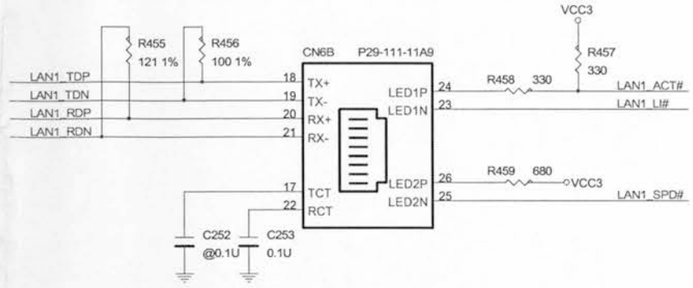
		EPoX COMPUTER CO., LTD			SCALE NONE	DRAWING DATE 2002-07-26	DRAWING TITLE D815E	Size A3	Description POWER	Rev. 0.0
		APPROVED MACRO	DESIGNED PING	DRAWN JOYCE	CUSTOMER NAME EPoX		JOB No. -	Sheet 19 of 21		

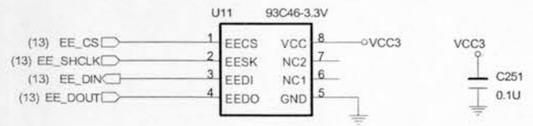


			EPoX COMPUTER CO., LTD		SCALE NONE	DRAWING DATE 2002-07-26	DRAWING TITLE D815E	Size A3	Description VRM_IRU3013	Rev. 0.0
			APPROVED MACRO	DESIGNED PING	DRAWN JOYCE	CUSTOMER NAME EPoX	JOB No. -	Sheet 20 of 21		









			EPoX COMPUTER CO., LTD		SCALE NONE	DRAWING DATE 2002-07-26	DRAWING TITLE D815E	Size A3	Description LAN1_82562EM	Rev. 0.0
			APPROVED MACRO	DESIGNED PING	DRAWN JOYCE	CUSTOMER NAME EPoX	JOB No. -	Sheet 21 of 21		

Exhibit A

M815A / ODM

Industrial ATX Board for Pentium® !!! Processor

Preliminary Specifications:

Processor: (Not Included)
- Intel® Celeron™ Processor with PPGA/FCPGA socket 370 packing: operating at 433 ~ 1.1GHz
- Intel® Pentium® !!! /Coppermine™ Processor with FC-PGA or FC-PGAII w/HIS. socket 370 packing: operating at 500MHz ~ 1.1GHz

Core Logic:
- Intel® 82815E

BIOS:
- Award BIOS

FSB:
- 100 / 133 MHz

Memory:
- Two 168-pins DIMM sockets, support up to 512MB

IDE:
- PIO Mode, DMA Mode and one channel for up to 2IDE Devices

LAN Controller:
- Onboard Intel 82562 EM 10/100 Base-TX Ethernet
- Onboard one RJ-45 connector

VGA function:
On-die Intel 815E chip integrated with 2D/3D graphic controller

USB:
- 2 x USB ports (Upper and lower, on Rear I/O)

Expansion Slots:
- 1 x 4XAGP slot

Golden finger :
- PCI signals according customer's assignment

Power connector :
- Power assignement provided by customer.

Environments:
- Operation temperature: 0°C to 60°C,
- Storage temperature: -20°C to 80°C,
- Relative humidity: 10% to 90% (Non-Condensing)

Dimensions (D x W):
- 190 mm x 187.01 mm
  Height according to 3D's drawing provided by customer.

Specification is subject to change accordiing to design concern Or customer's requirement.

Remarks :

1. Power is not existed with VCC5 SBY, VDIMM3, -12V & -5V.

2. PCI1 is not standard and not compatible.
   PCI1: B1, B2, B3,B4, A1, A2, A3, A4 will be VCC12
   PCI1: B5, B6, B7, B8, B9 will be respectively RST, BCLK, SDOUT, SDIN0, SYNC used for the AC97.
   PCI1: B10, B11, B12 will be respectively GPIO25, GPIO27, GPIO28.
   GAELCO will provide their PCI card for EPoX's validation.

3.JTAG of Pentium III connector is necessary.

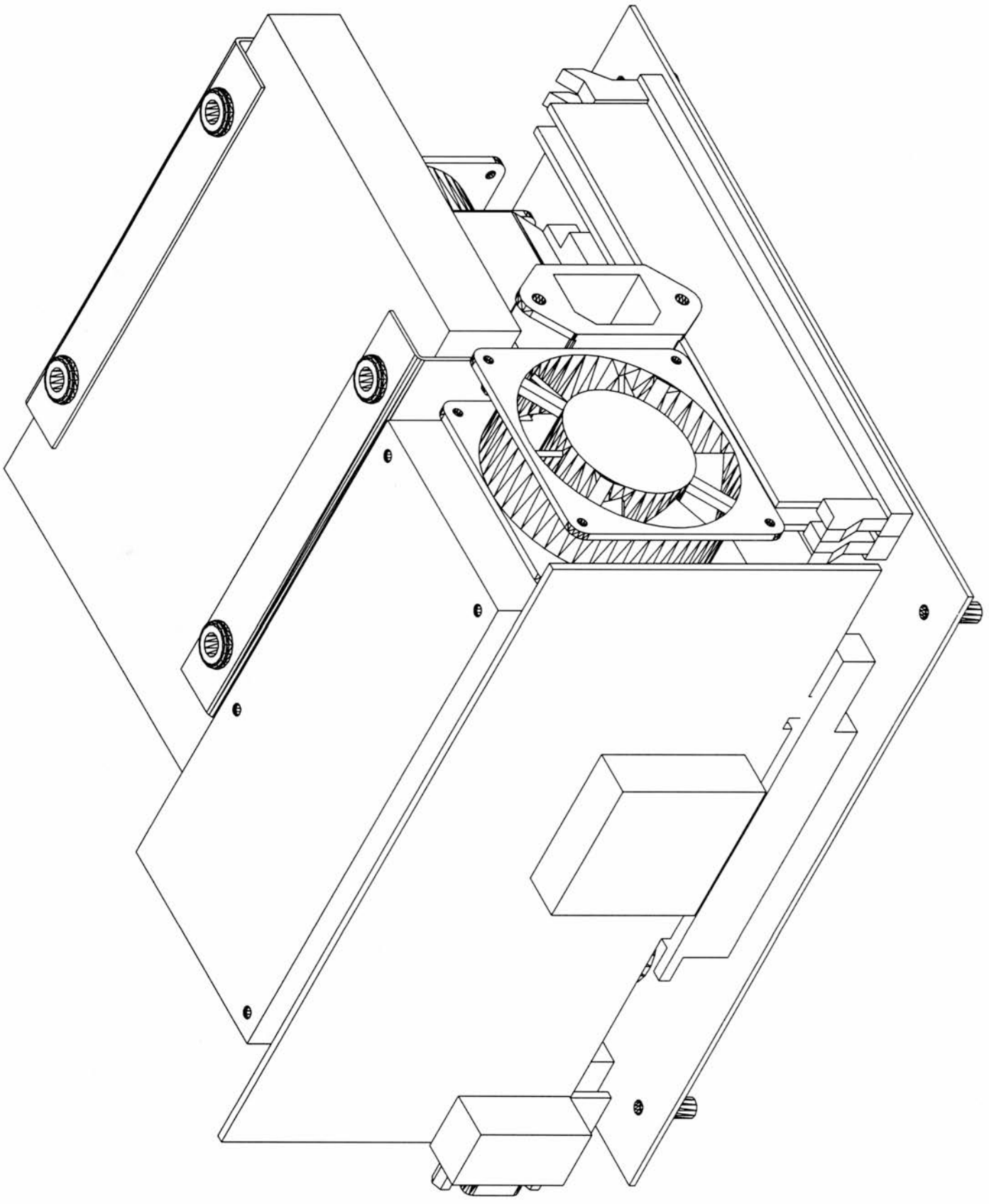
4. Operating system like Linux (Kernel 2.4.16) & Windows Embedded (Windows XP Kernel) will be modified by GAELCO and GAELCO also provide the finished OS for EPoX to test.

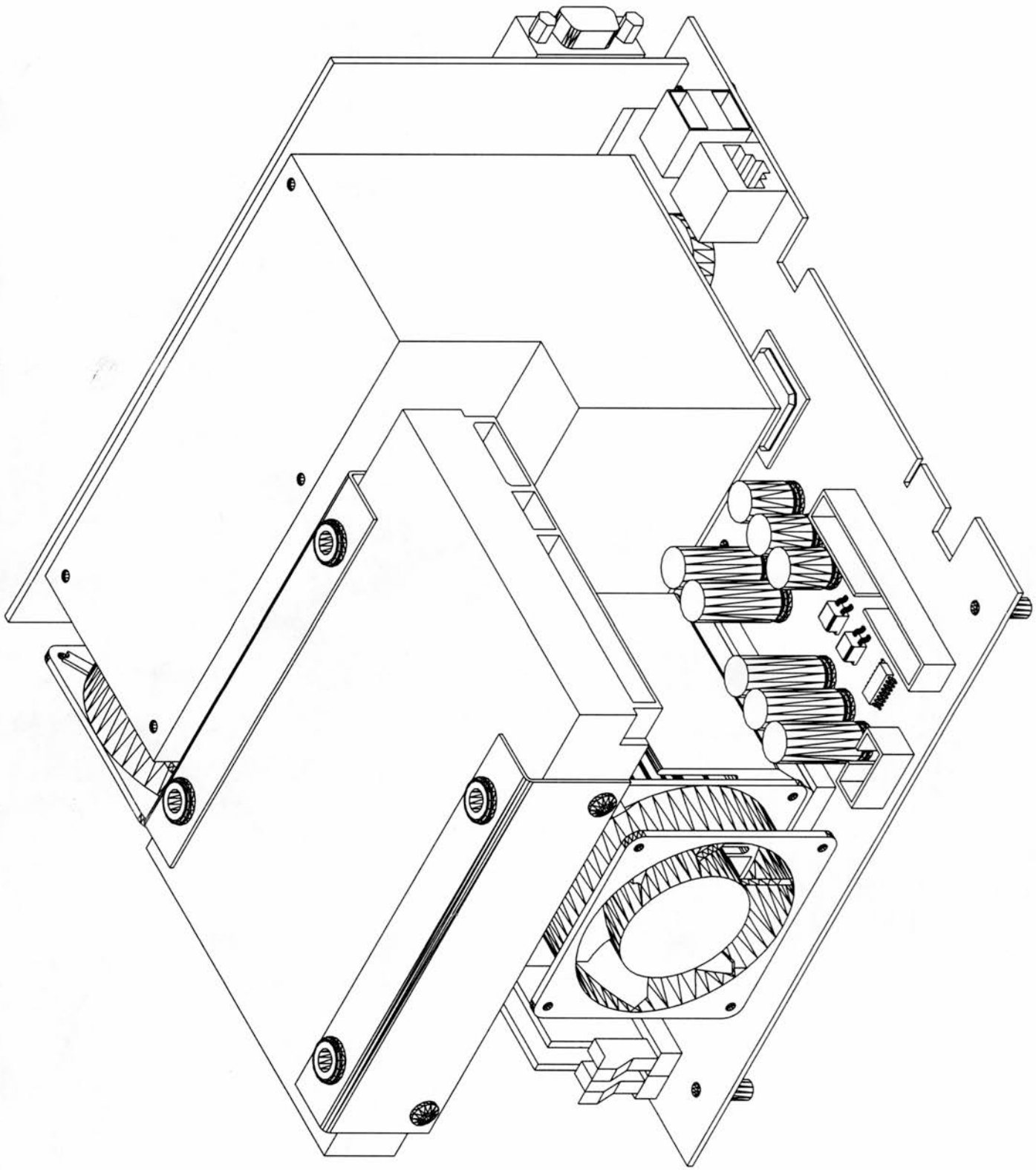
5. GAELCO will provide test program for EPoX to validate the ODM baord

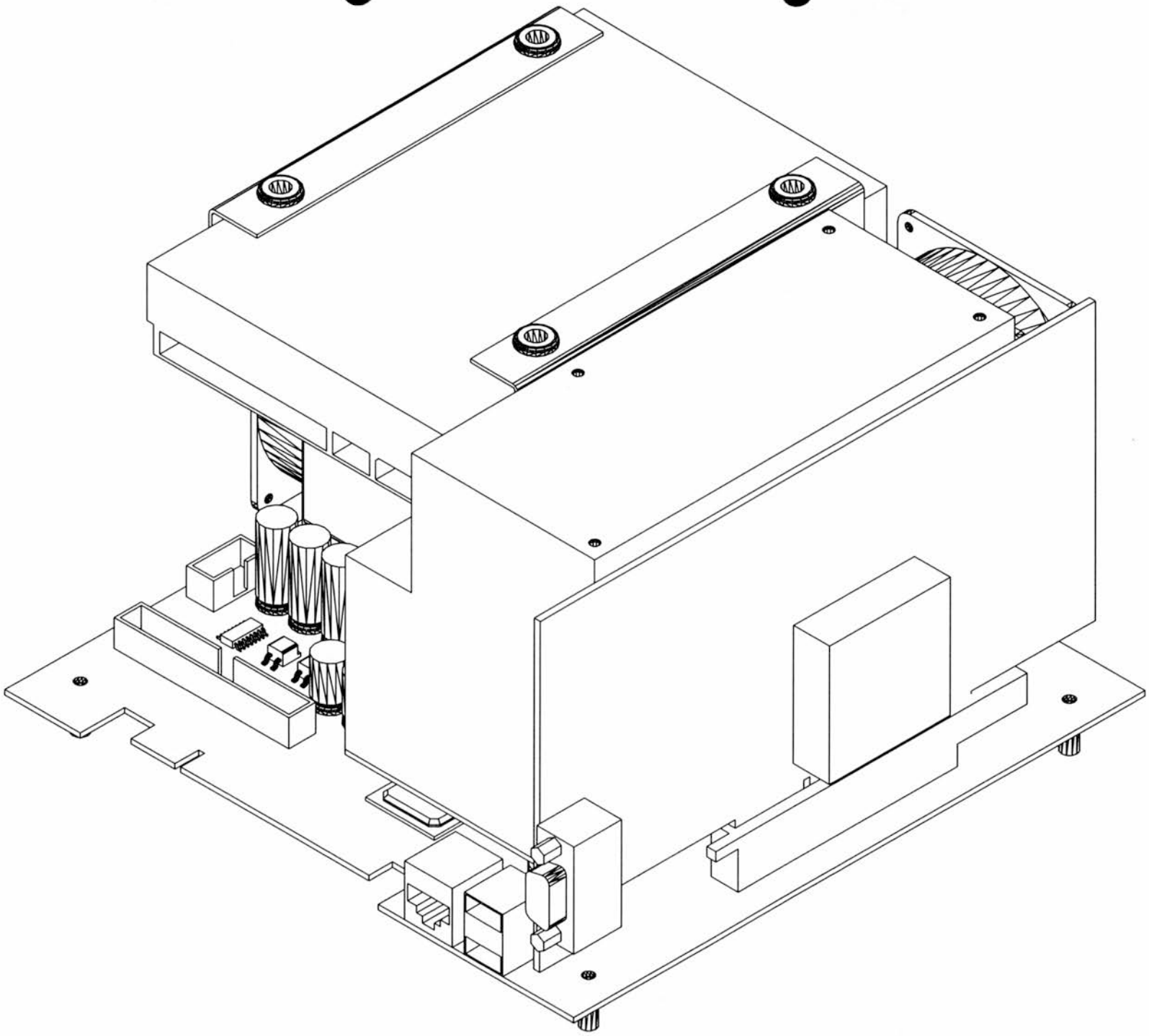
6. EPoX can modify the BIOS configuration in case it's required for any unsupported hardware changes. The NRE charge is US$ 4000.

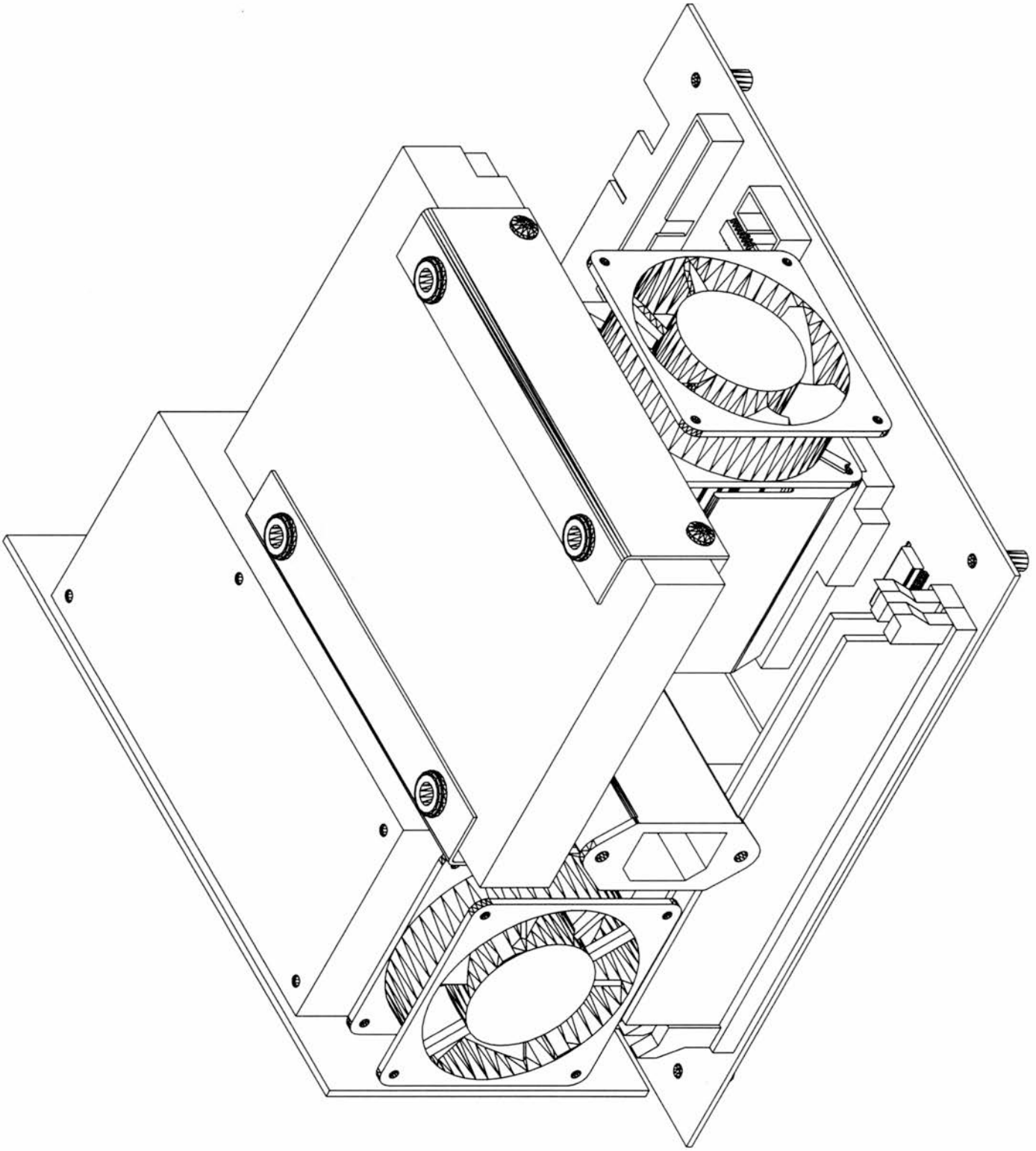
7. Only K/B is needed and will be connected through USB port.

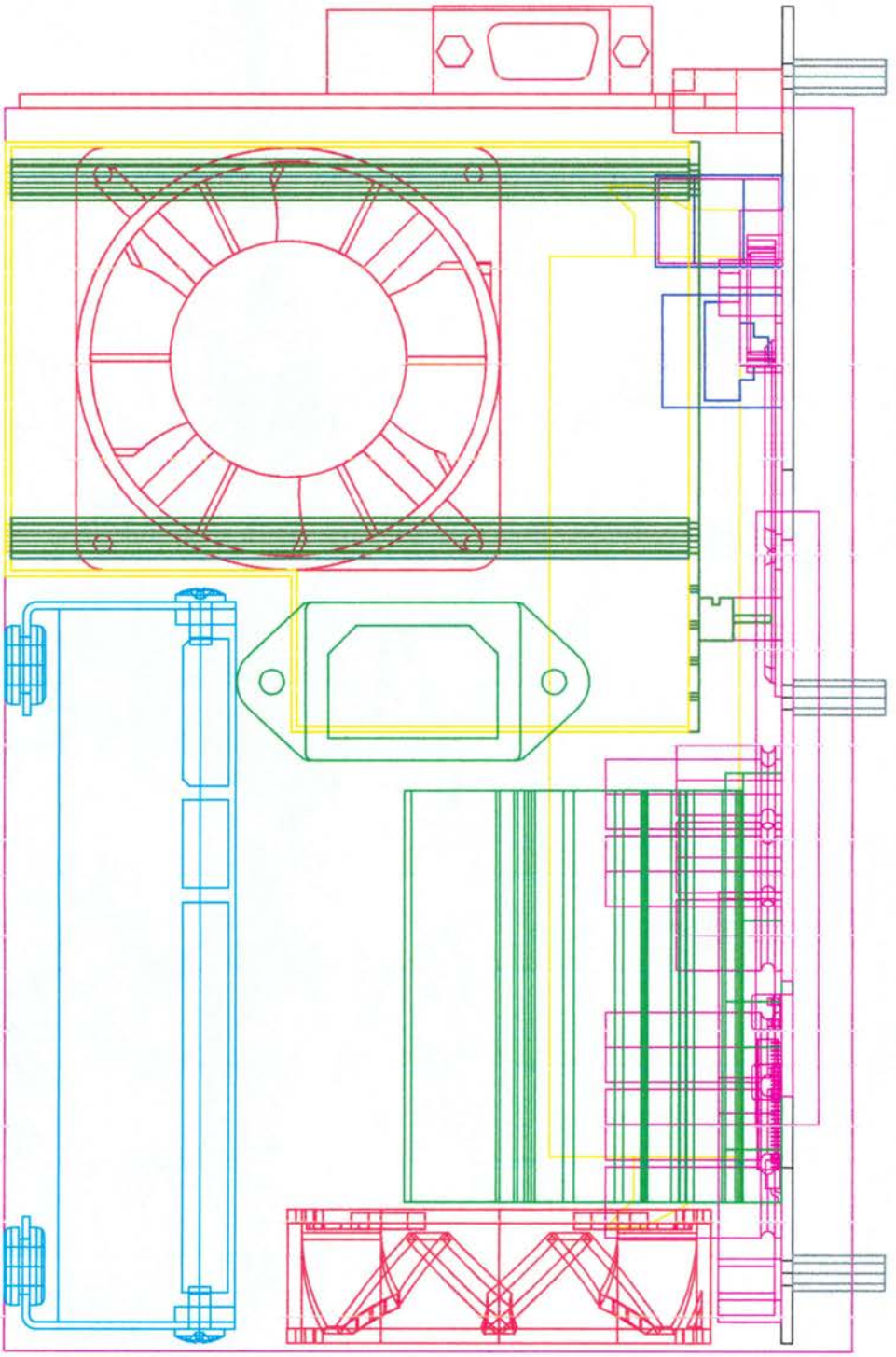
8. Customer will not need any block mechanism for the ODM board.

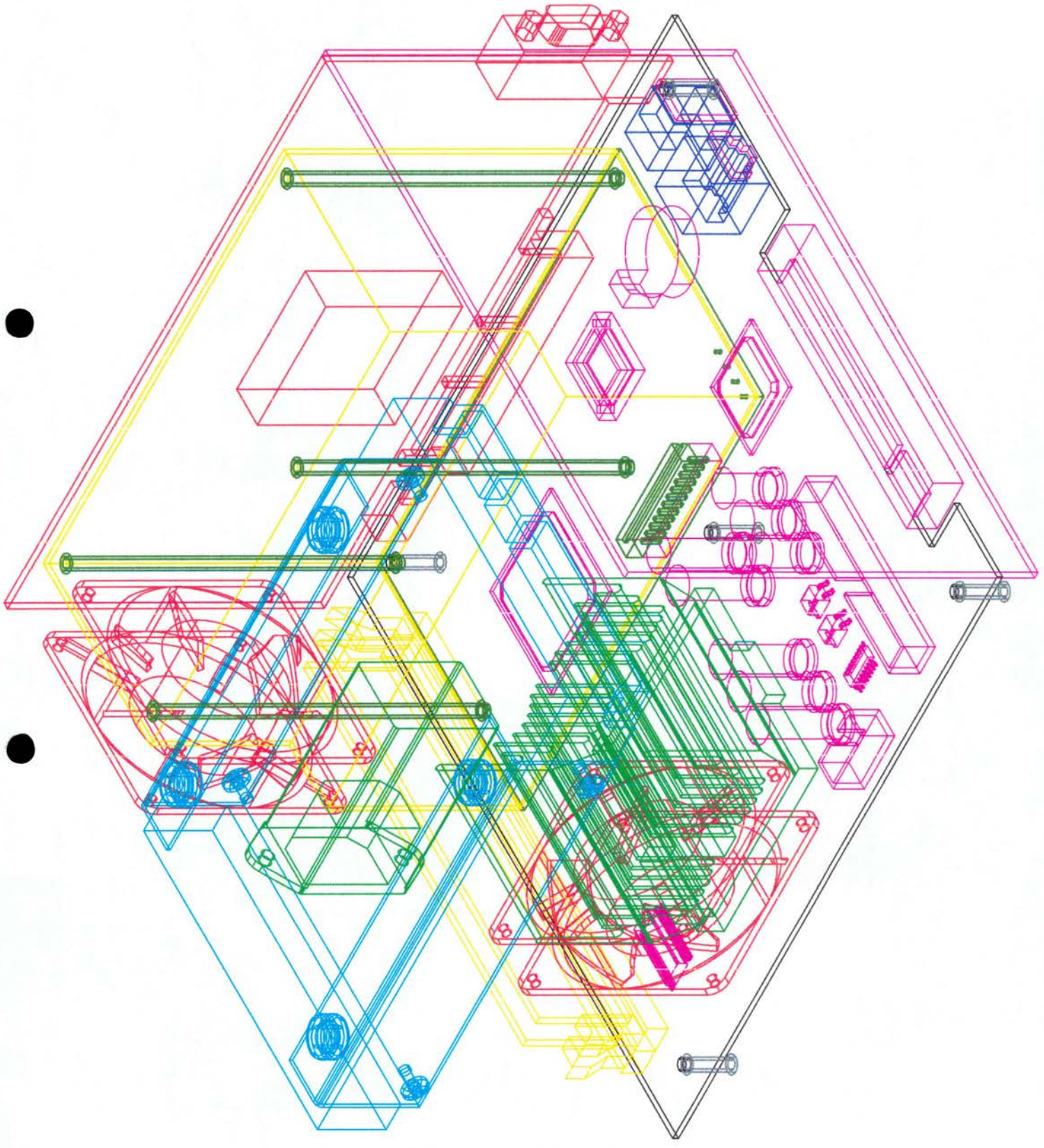


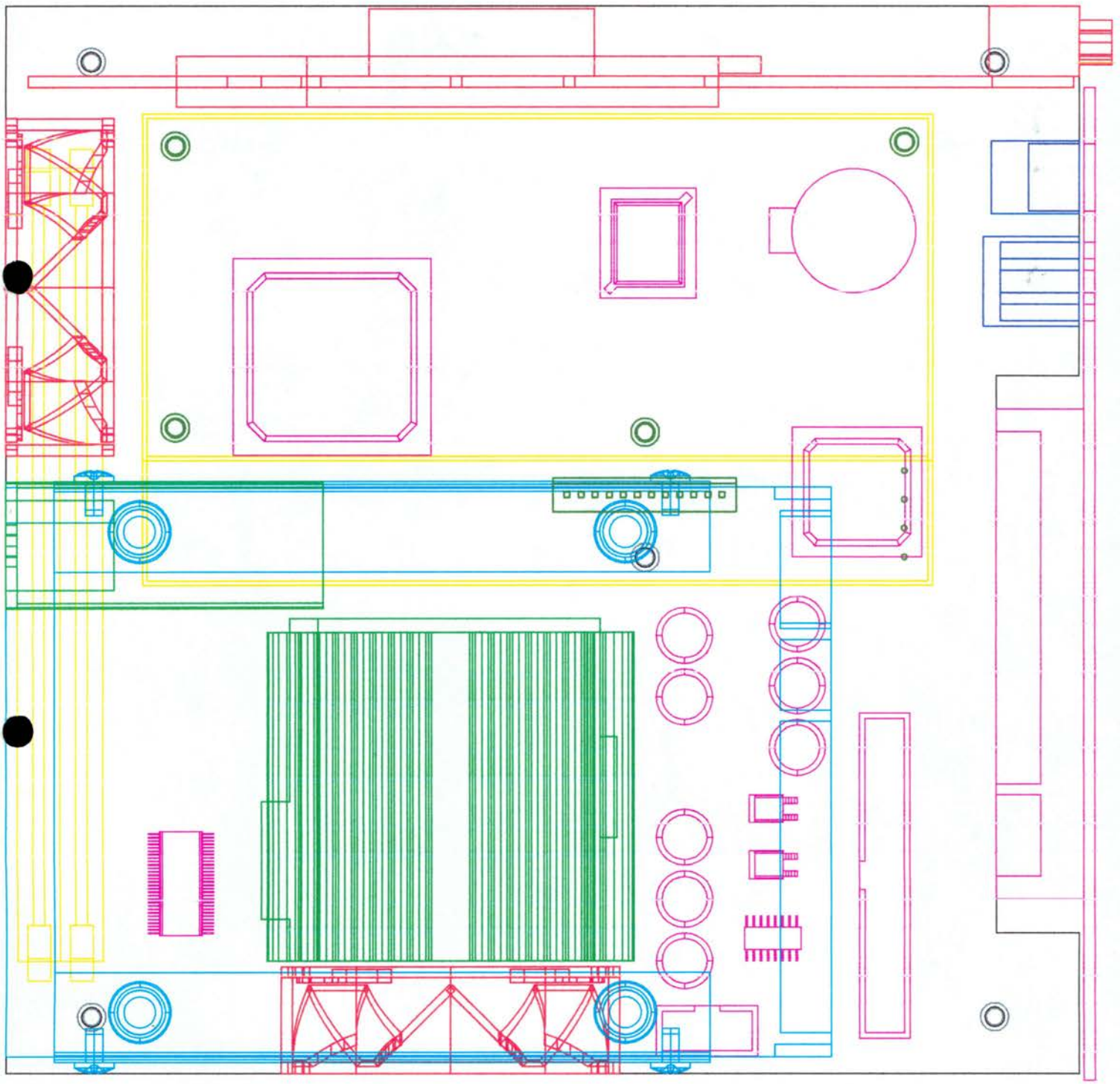


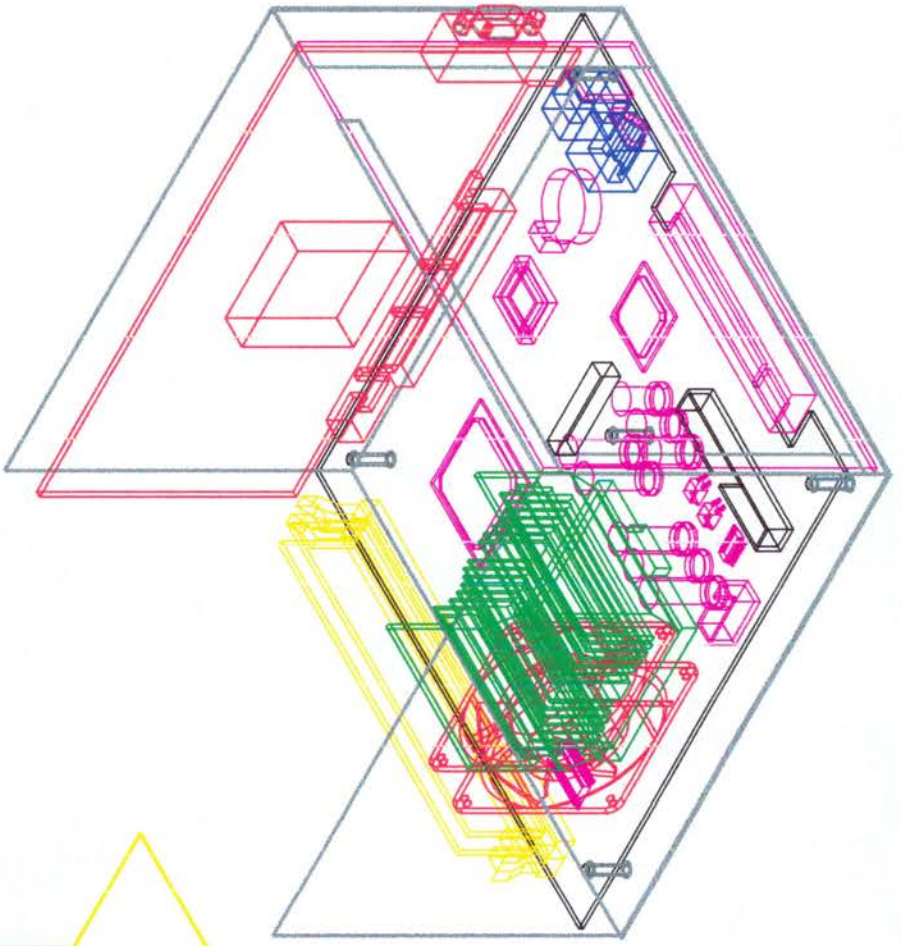


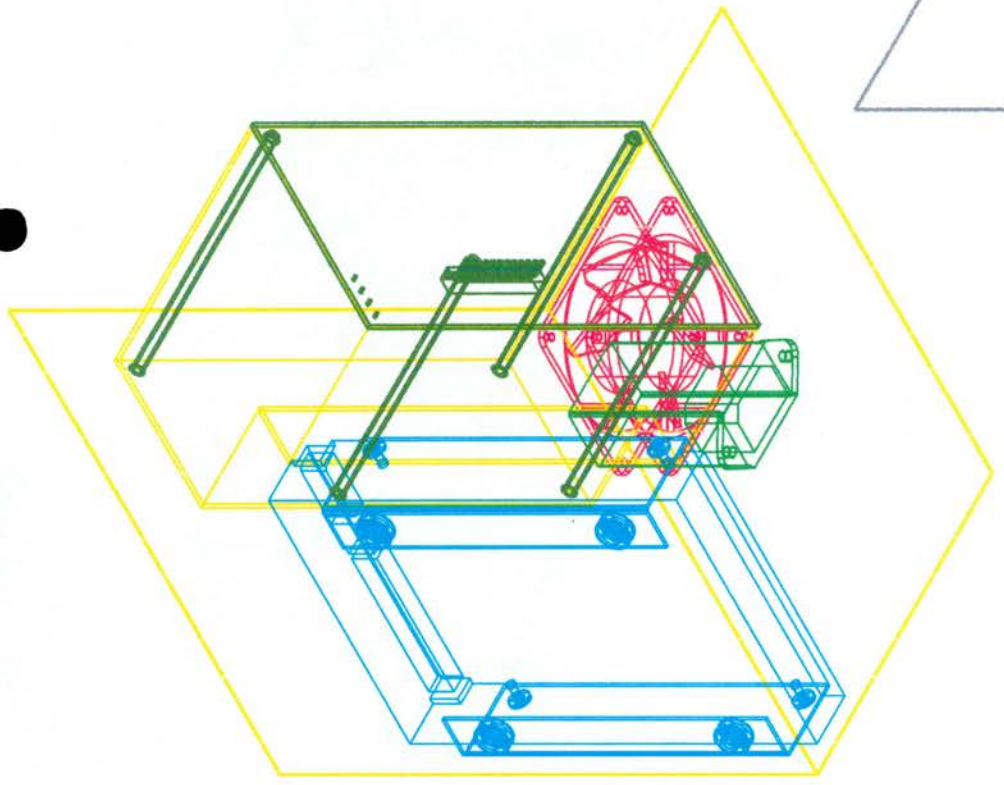


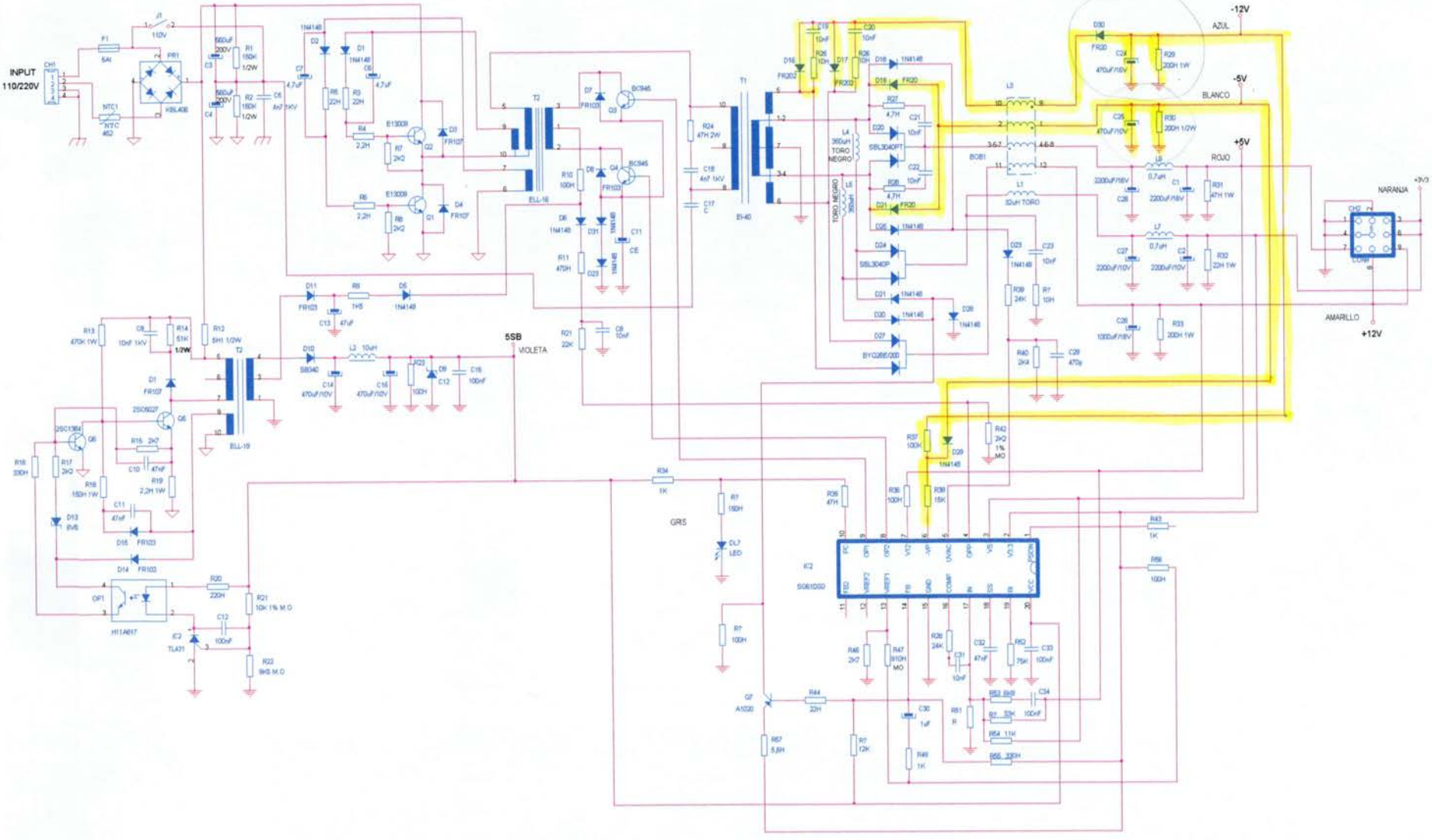


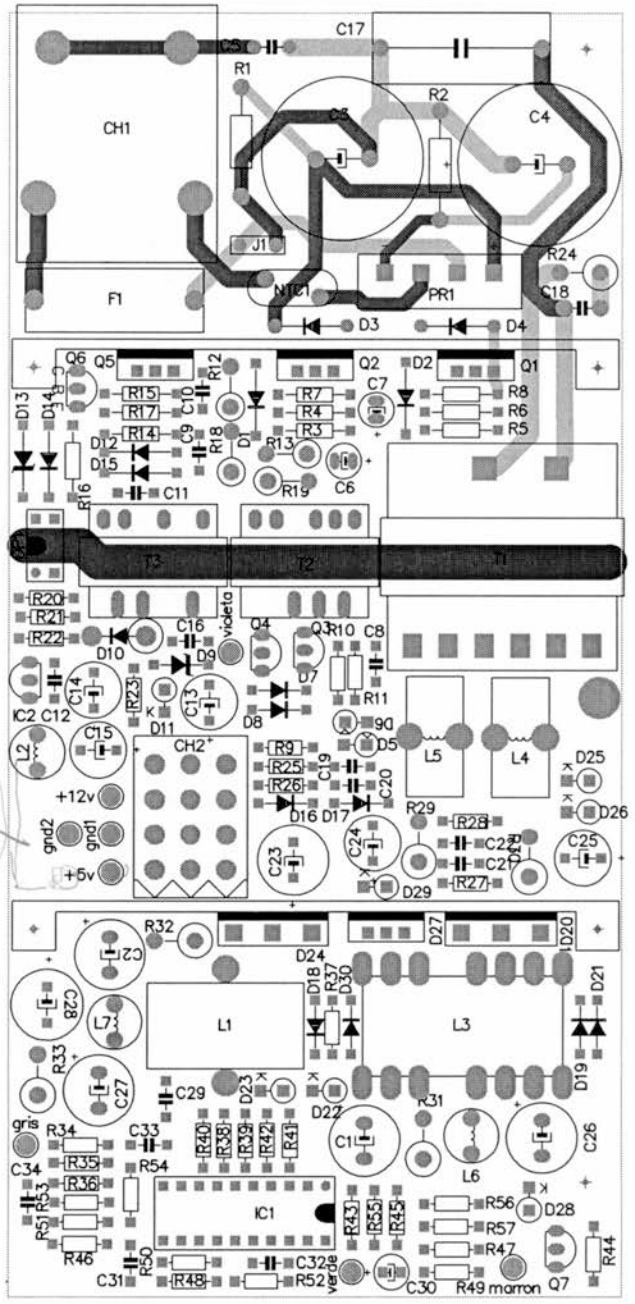






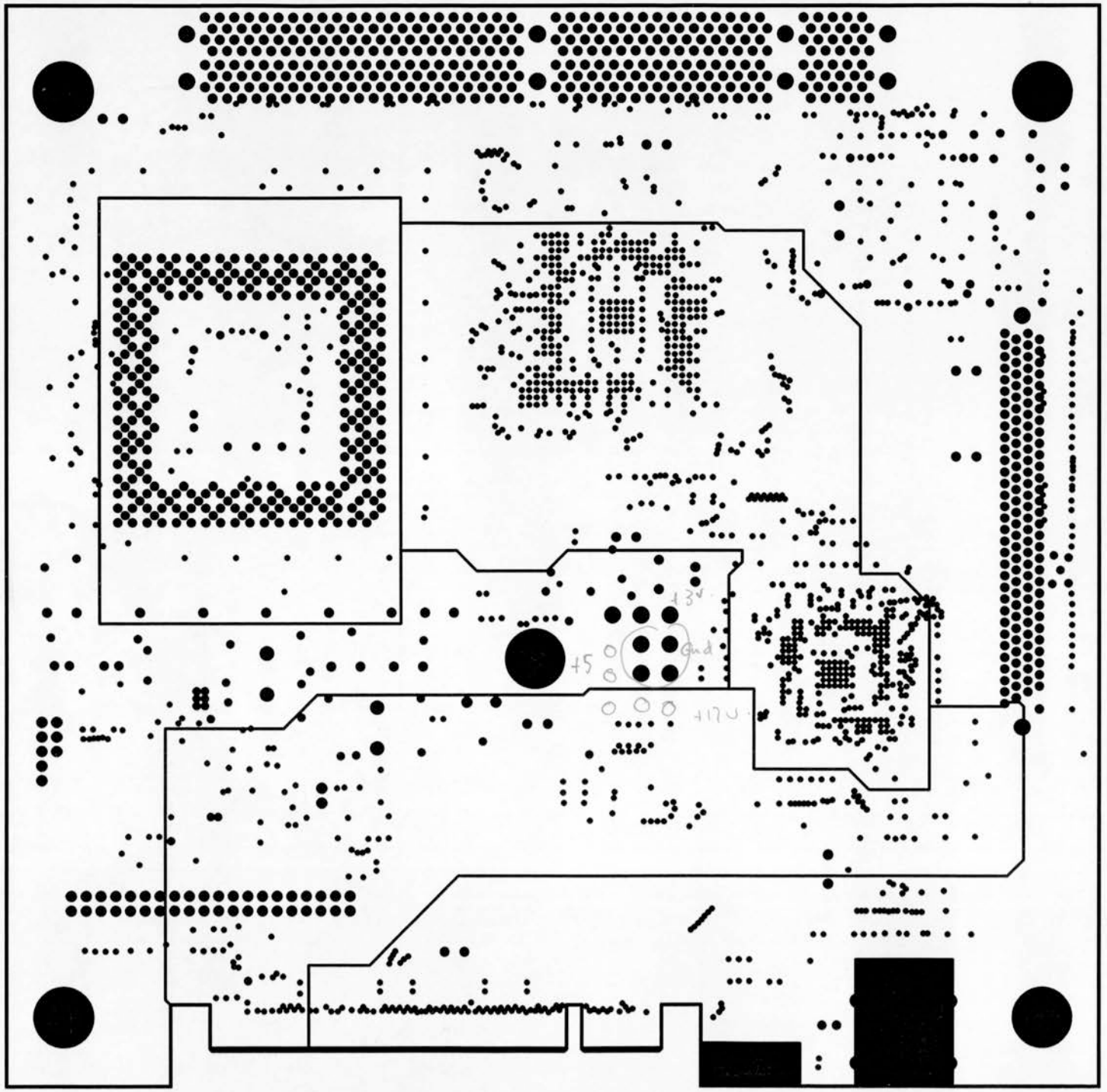


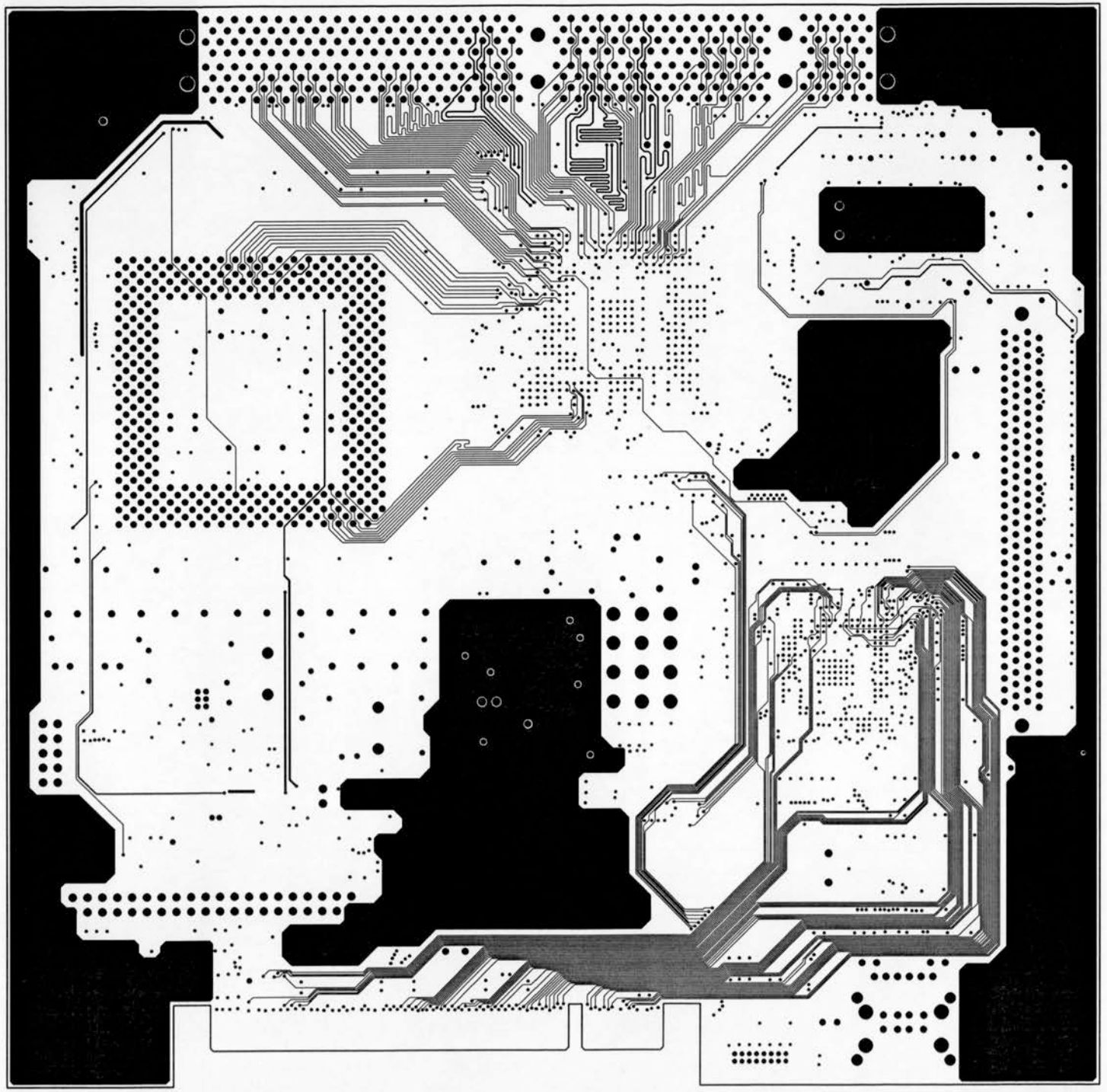

INPUT
110/220V
5SB
VIOLETA
GRIS
-12V
AZUL
-5V
BLANCO
+5V
ROJO
+3V3
NARANJA
AMARILLO
+12V
FONT GAELCO
FUENTE PC
JOSEP
Tuesday, December 31, 2002

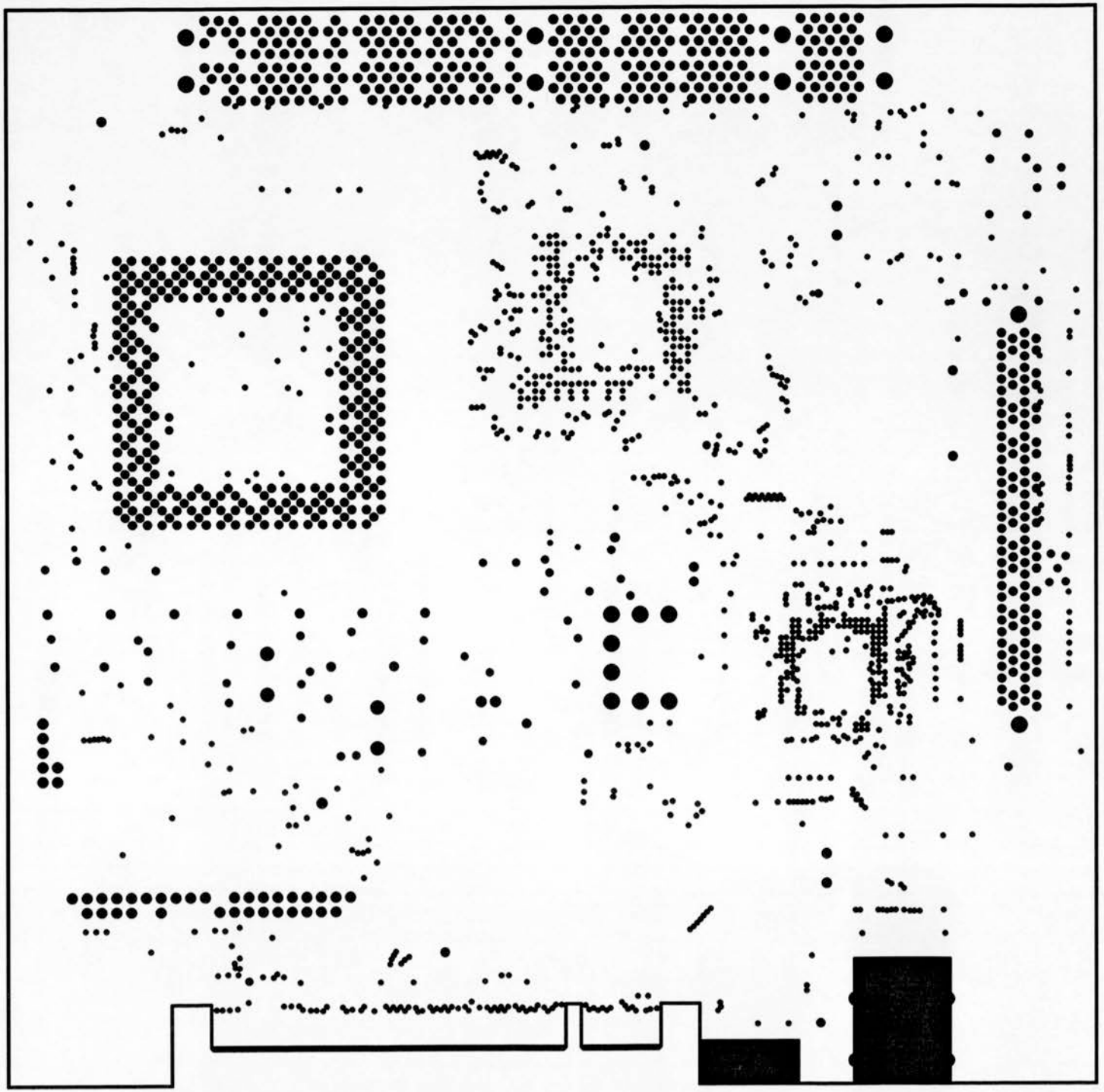


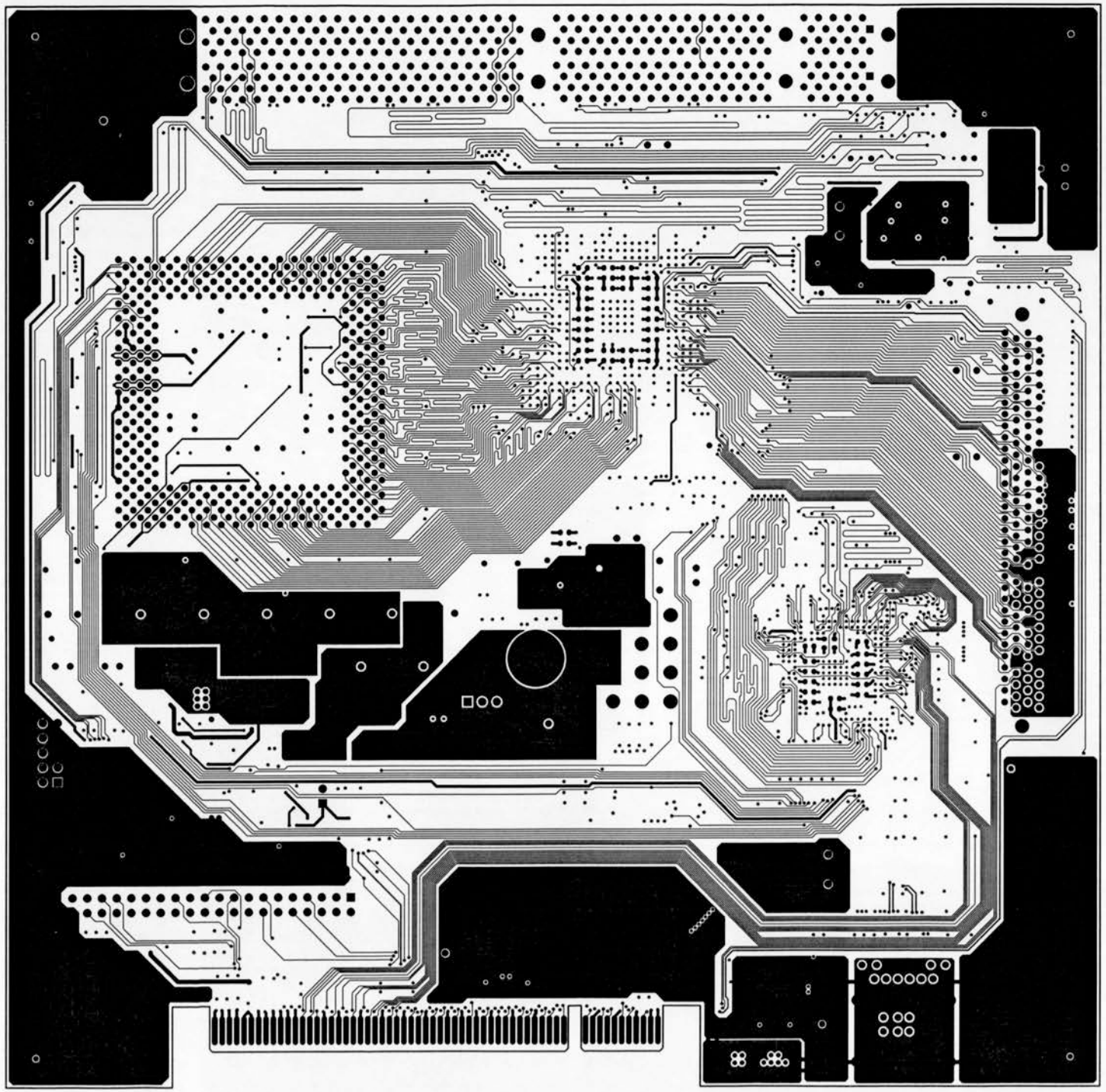
AERO43 160902

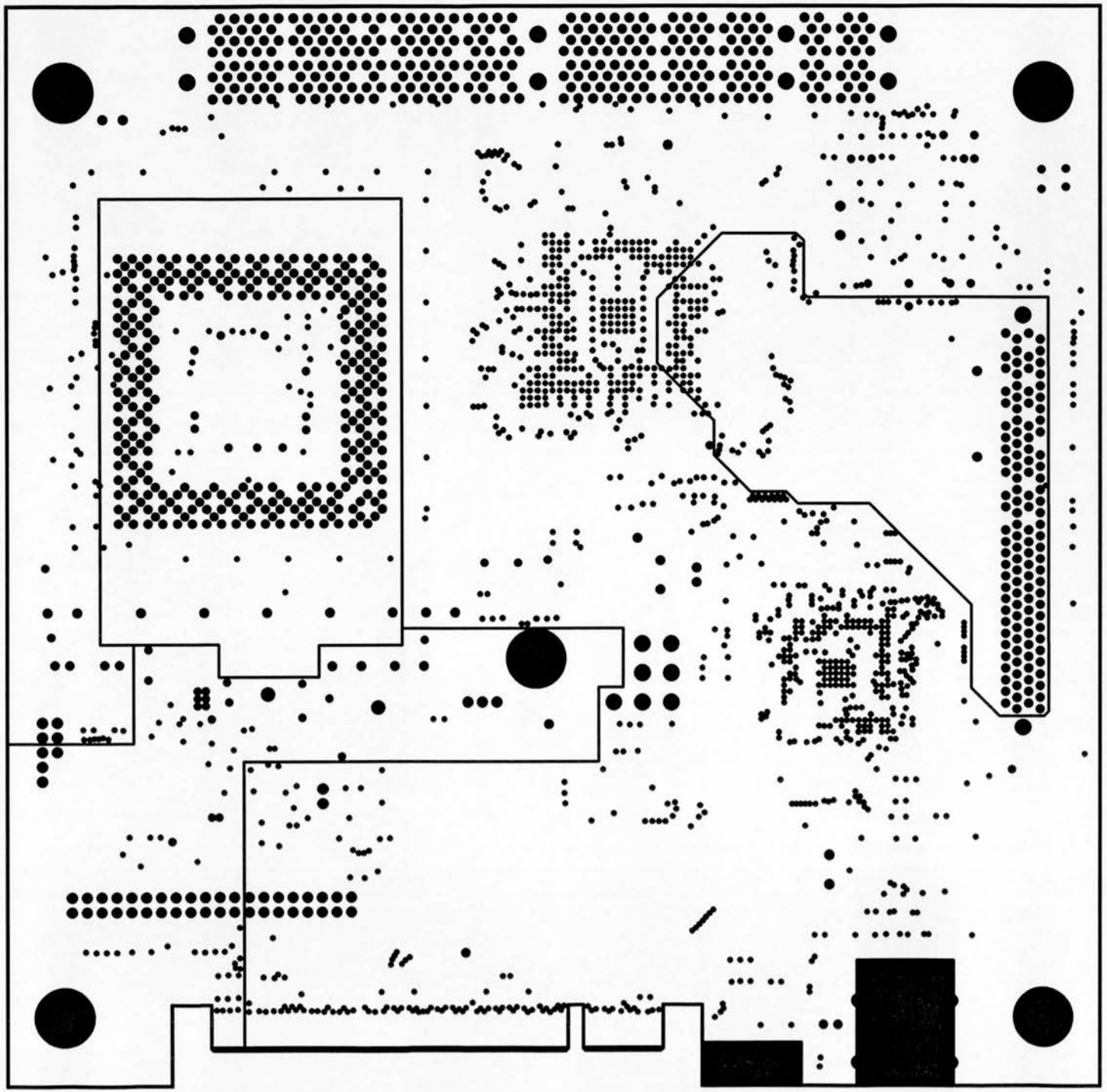
F. ALIMENTACION

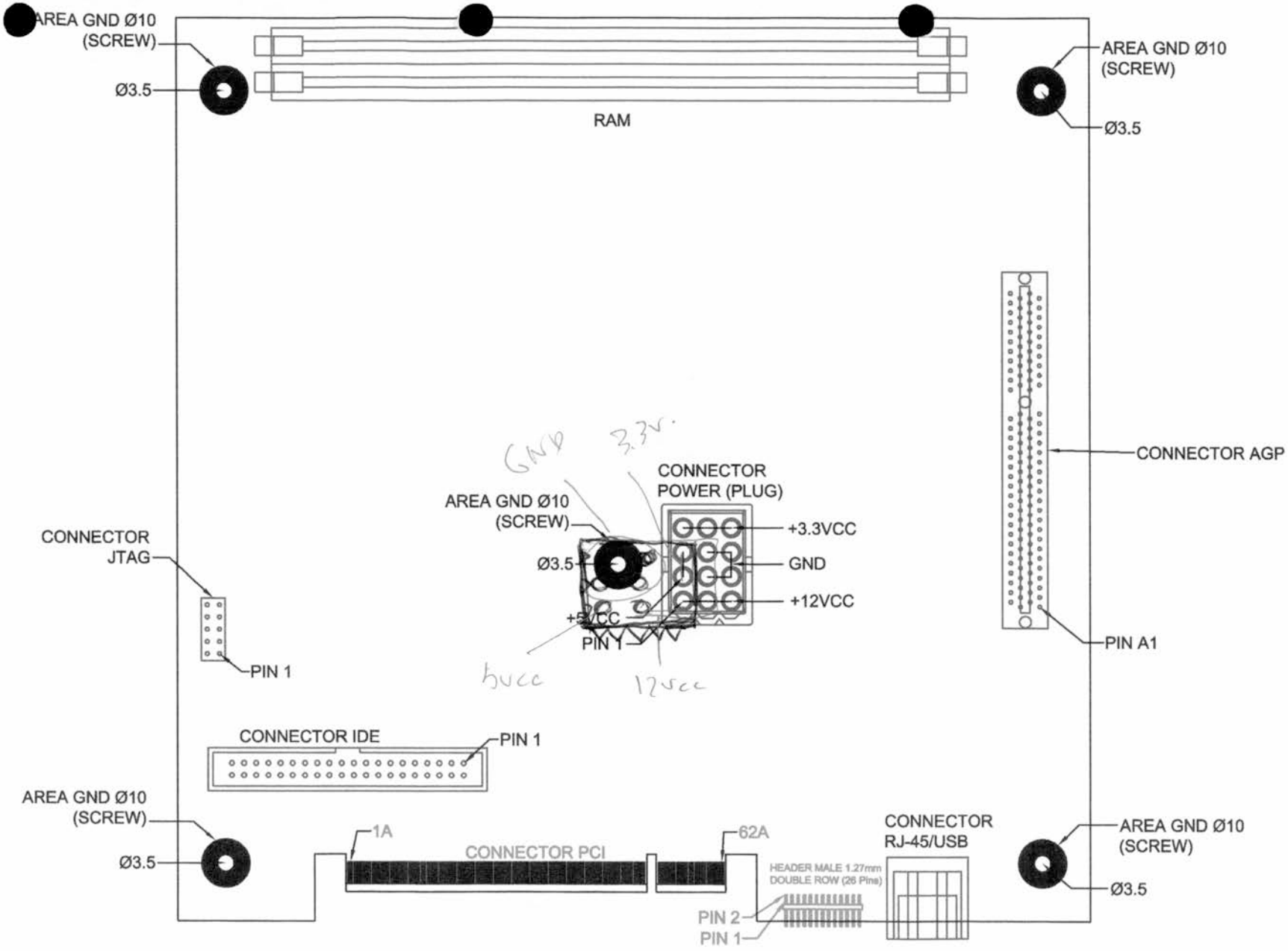

+3V
+5
Gnd
+12V











NOTA:
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS

Hardware specifications:

1- VCC5SBY voltage will be the same as VCC5. All SBY voltages will no exist. VDIMM3_3 voltage will be the same as VCC3.

2- VCC12- and VCC5M will no exist.

3- Power supply will be specific for this board and will be made by GAELCO.

4- We will only have PCI1, and it will be special (not standard and not compatible). It will include different pin configuration(see point 5 and 6). The PCI1 plug will be a card plug gold covered. The female for this connector will be placed in the frontal designed by GAELCO. (this means that the male/female will be in the inverse order compared with a common PC, where the female is placed in the mainboard). See schematics.

5-The following PCI1 pins will have the function of VCC12:
B1,B2,B3,B4,A1,A2,A3,A4.

6- The pins of PCI1: B6,B5,B7,B8,B9 will be respectively:
RST,BCLK,SDOUT,SDIN0,SYNC (to be used for the AC97), and pins B10,B11,B12 will be GPIO25,GPIO27,GPIO28 respectively.

7- LAN support will be adapted through a RJ45 connector and a Intel 82562EM chip.

8- Only two USB ports will be used: Upper and Lower.

9- W83627HF will be removed, because we don't need its ports and its floppy support.

10-We will include a JTAG connector for the PentiumIII to emulate the process

11- The mainboard power connector will be MOLEX model Order No.: 03-09-2121 and its pins will be MOLEX Part No.: 02-09-2134

12- We will only use primary IDE port, it the schemes is shown its place and orientation.

13- Microprocessor must be PentiumIII up to 1.2GHz or Celeron up to 1.2GHz. Both using socket 370

14- SDRAM sockets will be 168pins DIMM1 and DIMM2. We will use AGP 4X.

15- The mainboard must have a standard CPU fan connector (3 pins)

16- There will be no CMOS, its parameters will be inside FWH(BIOS)

17- We will not use W83628F, W83629D and XC9536XL chips, so we will not have any ISA bus.

18- The board will not have any EMIS filter, but its design will be optimized to minimize them.

19-We don't need AC'97 codec (it will be placed in the front board), we also don't need PRINTER PORT, GAME&MIDI, COM1, COM2, J5, J6.

20- The board does not need WDOG but we need a reset mini-switch and a checking chip that will notify when the 5VCC go below 4.68V (aprox.) (we cannot see this feature at the schemes). This chip must generate a reset when the voltage is low, and remove the reset if the voltage raises again. (Maybe this feature is included in IRU3013?)

21- We have added a new 26-pin VGA output connector (see attached scheme). This connector includes both Flat panel (digital) and CRT output. So the connector of your scheme 18/21 must be removed.

You can fix the pin distribution as you want in order to optimize the router of the main board. This connector must have the following pins:

-LTVDATA(0,11)
-LTVBLANK#
-LTVCLKOUT(0,1)
-TVVSYNC
-TVHSYNC
-LTVDA
-LTVCL
-VSYNC
-HSYNC
-RED
-GREEN
-BLUE
-AGND
-AGND

22- CNR SLOT is not necessary.

~~23- The board will include an output connector for the 815E built-in VGA.~~

24- RTC function of 82801 must be available an working, for this reason we need VCMOS voltage coming from a battery that we cannot see in your schemes. So this battery must be included

25- The placement of the CPU socket 370 can be fixed by your own in order to maintain standard spacing of the components (to avoid spacing problems with standard CPU cool radiators)

26- We think that 93C46 (U11 chip from scheme 21) is not necessary. Please, notify the reason to include it.

27- Regarding PCI gold finger: We are supposing that the A-pins are in the component side, and B-pins in the solder side. Please, notify if this is right.

Consideraciones del desarrollo

1° La tensión de VCC5SBY, será la misma que la VCC5. y todas las tensiones SBY no existirán, la tensión VDIMM3_3 será VCC3.
2° No tenedremos tension de VCC12- ni de VCC5M.
3° Los consumos serán VCC5_7,5A, VCC3_7,5A, VCC12_7,5A. y la tensión 110/220Vac
4° Los pines del PCI1 B1,B2,B3,A1,A2,A3,A4, pasarán a tener la función de VCC12.
5° Los pines del PCI1 B4,B14,A9,A11,A14 serán RST,BCLK,SDOUT,SDIN0,SYNC del AC97 respectivamente, y los B9,B10,B11 serán GPIO25,GPIO27,GPIO28, libres.
6° Adaptaremos la LAN para ETHERNET 10/100, con un conector J45 con el nuevo chip de INTEL.
7° Tendremos dos USB ports el Upper y el Lower.
8° Tendremos una adaptacion del bus PCI de carta en el circuito principal y el conector en el panel frontal.
9° Si se puede suprimir el W83627HF el KEYBOERD entrará por un USB, si no el conector PS2 MOUSE y el KEYBOARD estaran en el circuito camuflados. No hace falta que se protejan contra EMIS.
10° Pondremos un conector JTAG del PENTIUM III para emular el procesador.
11° El conector de la fuente irá transversal y tanto la hembra como el macho iran soldados a sus circuitos.
12°. Del circuito de la fuente saldran los cables para alimentar el disco duro, con el conector estandar (IDE primario).
13° Solo tendremos el bus IDE_PRIMARIO orientado y situado en su lugar
14° El pentium III debe ser FC-PGAII w/IHS o bien el FC-PGA.
15° Los zocalos de SDRAM serán DIMM1 y DIMM2 de 168 PIN y conservaremos el AGPX4.
16° El ventilador del procesador deberia ir lateral, expulsando aire al exterior con lo cual el radiador sera diferente y el zocalo no debe ser necesariamente de inserción zero.
17° El ventilador de la fuente expulsará aire al exterior
18° Debemos prescindir de la CMOS, W83628F, W83629D, XC9536XL.
19° Los parametros de la CMOS estaran definidos en el FWH (BIOS)
20° Situar el conector de alimentación y el selector de 220/110 VAC en su sitio.
21° La fuente llevará un filtro de conducidas hasta 30Mhz, las frecuencias superiores las filtraremos al traspasar el chasis con otro filtro.
22° El panel frontal lo realizará GAELCO.
23° EL Codec'97 irá en la placa frontal junto con los amplificadores.
24° No necesitamos AC'97Codec, PRINTER PORT, GAME & MIDI, COM1, COM2, J5, J6.
25° La placa no necesita WDOG pero si un micro pulsador de RESET.
26° El conector de SVGA saldrá directamente de la tarjeta aceleradora.
27° El chip MCH no hace falta que lleve la versión para VGA.
28° El sistema operativo será un LINUX modificado por GAELCO para correr en tiempo real.

13/03/2002

Hardware specifications:

1- VCC5SBY voltage will be the same as VCC5. All SBY voltages will no exist. VDIMM3_3 voltage will be the same as VCC3.

2- VCC12- and VCC5M will no exist.

3- Power supply will be specific for this board and will be made by GAELCO.

4- We will only have PCI1, and it will be special (not standard and not compatible). It will include different pin configuration(see point 5 and 6). The PCI1 plug will be a card plug gold covered. The female for this connector will be placed in the frontal designed by GAELCO. (this means that the male/female will be in the inverse order compared with a common PC, where the female is placed in the mainboard). See schematics.

5-The following PCI1 pins will have the function of VCC12: B1,B2,B3,B4,A1,A2,A3,A4.

6- The pins of PCI1: B6,B5,B7,B8,B9 will be respectively: RST,BCLK,SDOUT,SDIN0,SYNC (to be used for the AC97), and pins B10,B11,B12 will be GPIO25,GPIO27,GPIO28 respectively.

7- LAN support will be adapted through a RJ45 connector and a Intel 82562EM chip.

8- Only two USB ports will be used: Upper and Lower.

9- W83627HF will be removed, because we don't need its ports and its floppy support.

10-We will include a JTAG connector for the PentiumIII to emulate the process

11- Power connector between power supply board (male) and main board (female) must be defined (both connectors must be to mount over PCB, not wires).

12- We will only use primary IDE port, it the schemes is shown its place and orientation.

13- PentiumIII must be FC-PGAII w/IHS or FC-PGA

14- SDRAM sockets will be 168pins DIMM1 and DIMM2. We will use AGP 4X.

15- We will use only the Pentium cool fan, that will go with a fixed 12VCC plug.

16- There will be no CMOS, its parameters will be inside FWH(BIOS)

17- We will not use W83628F, W83629D and XC9536XL chips, so we will not have any ISA bus.

18- The board will not have any EMIS filter, but its design will be optimized to minimize them.

19-We don't need AC'97 codec (it will be placed in the front board), we also don't need PRINTER PORT, GAME&MIDI, COM1, COM2, J5, J6.

20- The board does not need WDOG but we need a reset mini-switch and a checking chip that will notify when the 5VCC go below 4.68V (aprox.)

21- The MCH chip will have VGA function built-in

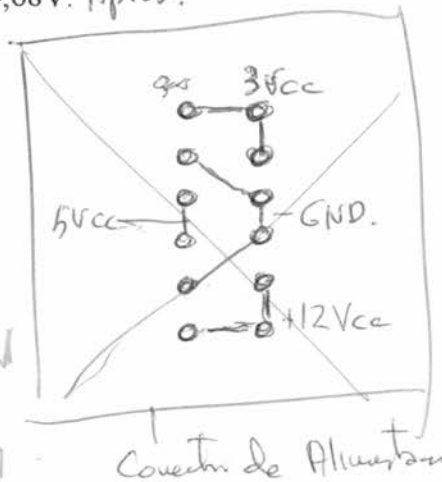
22- CNR SLOT is not necessary.

23- The board will include an output connector for the 815E built-in VGA.

Consideraciones HARDWARE

1° La tensión de VCC5SBY, será la misma que la VCC5. y todas las tensiones SBY no existirán, la tensión VDIMM3_3 será VCC3.
2° No tenedremos tension de VCC12- ni de VCC5M.
3° La fuente sera especial para esta placa y en principio la realizará GAELCO.
4° Solo tendremos el **PCI1**, y será especial (no estandar ni compatible), a parte de tener los pines diferentes (definidos en los apartados 4° y 5°) el conector **PCI1** sera de carta bañado en oro en el circuito principal, y en el panel frontal que realizará GAELCO, se pondrá el conector (ver graficos del sistema mecanico).
5° Los pines del **PCI1** B1, B2, B3, A1, A2, A3, A4, pasarán a tener la función de VCC12.
6° Los pines del **PCI1** ~~B4, B14, A9, A11, A14~~ serán RST, BCLK, SDOUT, SDIN0, SYNC del AC97 respectivamente, y los ~~B9, B10, B11~~ serán GPIO25, GPIO27, GPIO28.
7° Adaptaremos la LAN para ETHERNET 10/100, con un conector RJ45 y el chip de INTEL 82562EM.
8° Tendremos solo dos USB ports el Upper y el Lower.
9° Se suprimirá el W83627HF , puesto que no necesitamos ningun port ni el floppy disc.
10° Pondremos un conector JTAG del PENTIUM III para emular el procesador.
11° Debemos definir el tipo de conector de alimentacion para que sea el macho y la hembra para soldadura en PCB.
12° Solo tendremos el bus IDE_PRIMARIO orientado y situado en su lugar según graficos.
13° El pentium III debe ser FC-PGAII w/IHS o bien el FC-PGA.
14° Los conectores de SDRAM serán DIMM1 y DIMM2 de 168 PIN y conservaremos el AGPX4.
15° Solo habrá el ventilador del PENTIUM que ira con un conector a 12VCC fijo.
16° No habrá CMOS y los parametros estarán definidos en la FWH (BIOS).
17° Debemos prescindir de los chips, W83628F, W83629D, XC9536XL y por lo tanto no tendremos ningun bus ISA.
18° No tendra la placa ningun filtro especial para las EMIS, pero si que el diseño estará optimizado para minimizarlas.
19° No necesitamos AC'97Codec (irá en el frontal), ni tampoco el PRINTER PORT, GAME & MIDI, COM1, COM2, J5, J6.
20° La placa no necesita WDOG pero si un mini pulsador de RESET y un chip SUPERVISOR para cuando los 5VCC bajan por debajo de 4,68V. Aprox.
21° El chip MCH no hace falta que lleve la versión para VGA.
22° El CNR SLOT no es necesario.

28/05/2002

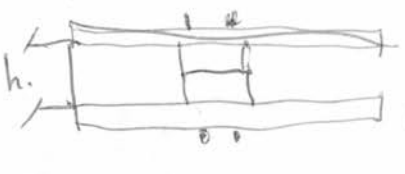


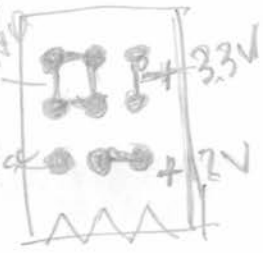
Conector de Alimentacion

4 ~~7~~
2 +5Vcc
3 +3.3Vcc
3 +12Vcc

Conector de 12Vcc, 5Amp/Vcc. Circuito/Circuito

~~Lo mas alto~~
como mas alto mejor (h. → max.)





REFUNDIDO DE ESPECIFICACIONES

CAMBIOS A PARTIR DE LOS ESQUEMAS Rev 0.1 2002-09-26

1°- El conector de alimentación se ha reducido a 9 pins y se ha desplazado, ver posicionamiento en graficos. El fabricante y el modelo sigue siendo el mismo.

2°- El conector de video digital pasa a ser el modelo xxxxxx y tendra la distribución siguiente.

Pin 1a	RED	Pin 1b	GREEN
Pin 2a	BLUE	Pin 2b	VSYNC
Pin 3a	HSYNC	Pin 3b	GND
Pin 4a	GND	Pin 4b	LTVDATA0
Pin 5a	LTVDATA3	Pin 5b	LTVDATA2
Pin 6a	LTVDATA1	Pin 6b	LTVDATA4
Pin 7a	LTVDATA5	Pin 7b	LTVDATA6
Pin 8a	LTVDATA7	Pin 8b	LTVDATA8
Pin 9a	LTVDATA9	Pin 9b	LTVDATA10
Pin 10a	LTVDATA11	Pin 10b	LTVBLANK
Pin 11a	LTVCLKOUT0	Pin 11b	LTVCLKOUT1
Pin 12a	TVVSYNC	Pin 12b	TVHSYNC
Pin 13a	LTVDA	Pin 13b	LTVCL

3°- El conector JTAG del PROCESADOR no hace falta montarlo en las placas.

4°- La placa usará la CMOS del RTC, si se saca la bateria se cargarán los parametros estandar que estan almacenados en la BIOS.

5°- La BIOS después de inicializar el B0:D30:F0 (GPIO) y antes del B0:D30:F0, debemos ejecutar un modulo de BIOS para inicializar la circuiteria que tenemos en el GOLD_FINGER. El codigo binario lo suministrará GAELCO. Este modulo residirá en la BIOS.