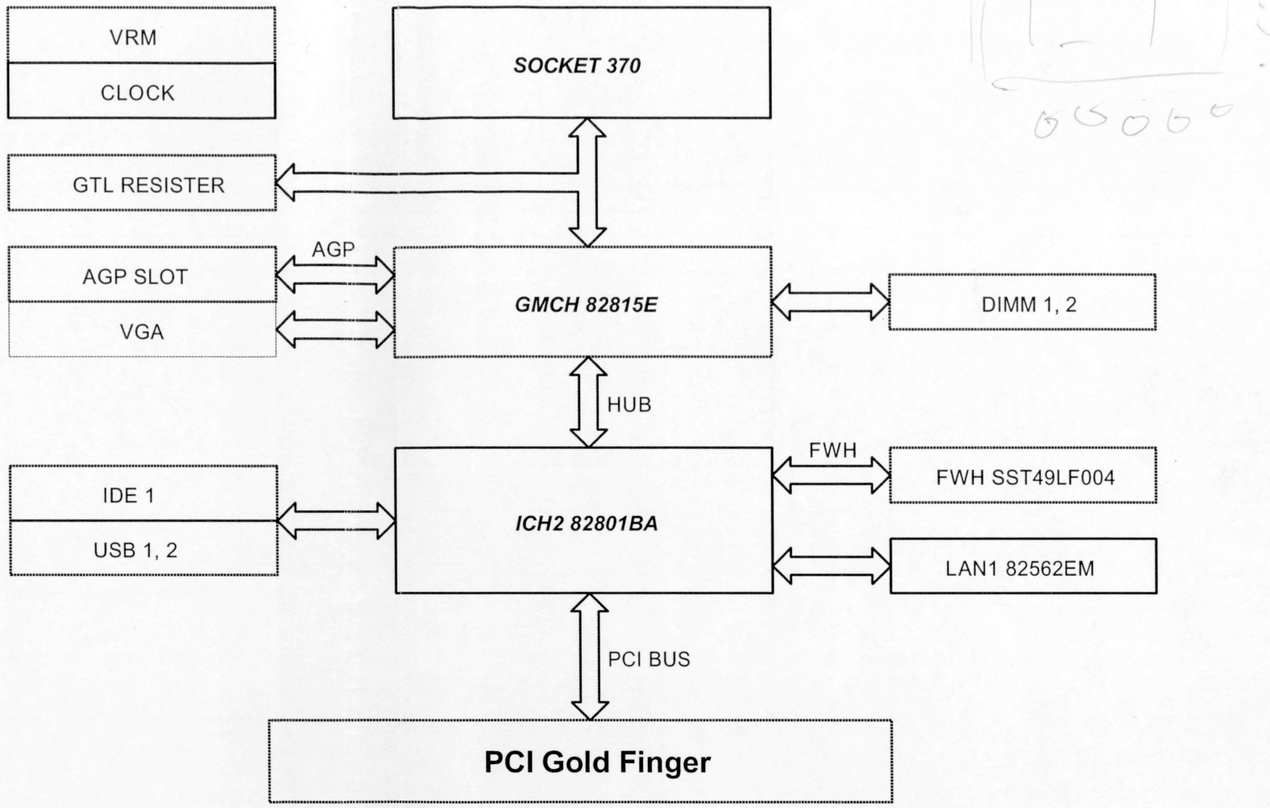
D815E

01	COVER SHEET
02	SOCKET370 1/2
03	SOCKET370 2/2
04	GTL RESISTER
05	CLOCK SYNTESIZER
06	GMCH_82815E 1/3
07	GMCH_82815E 2/3
08	GMCH_82815E 3/3
09	AGP SLOT
10	DIMM 1/2
11	DIMM 2/2
12	ICH2_82801BA 1/2
13	ICH2_82801BA 2/2
14	FWH
15	IDE CONNECTOR
16	USB PORT
17	PCI GF
18	VGA CONNECTOR
19	POWER
20	VRM_IRU3013
21	LAN1_82562EM

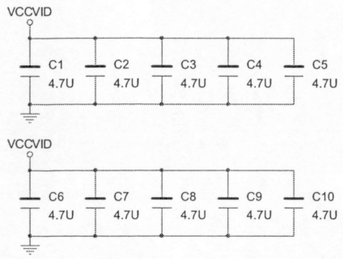


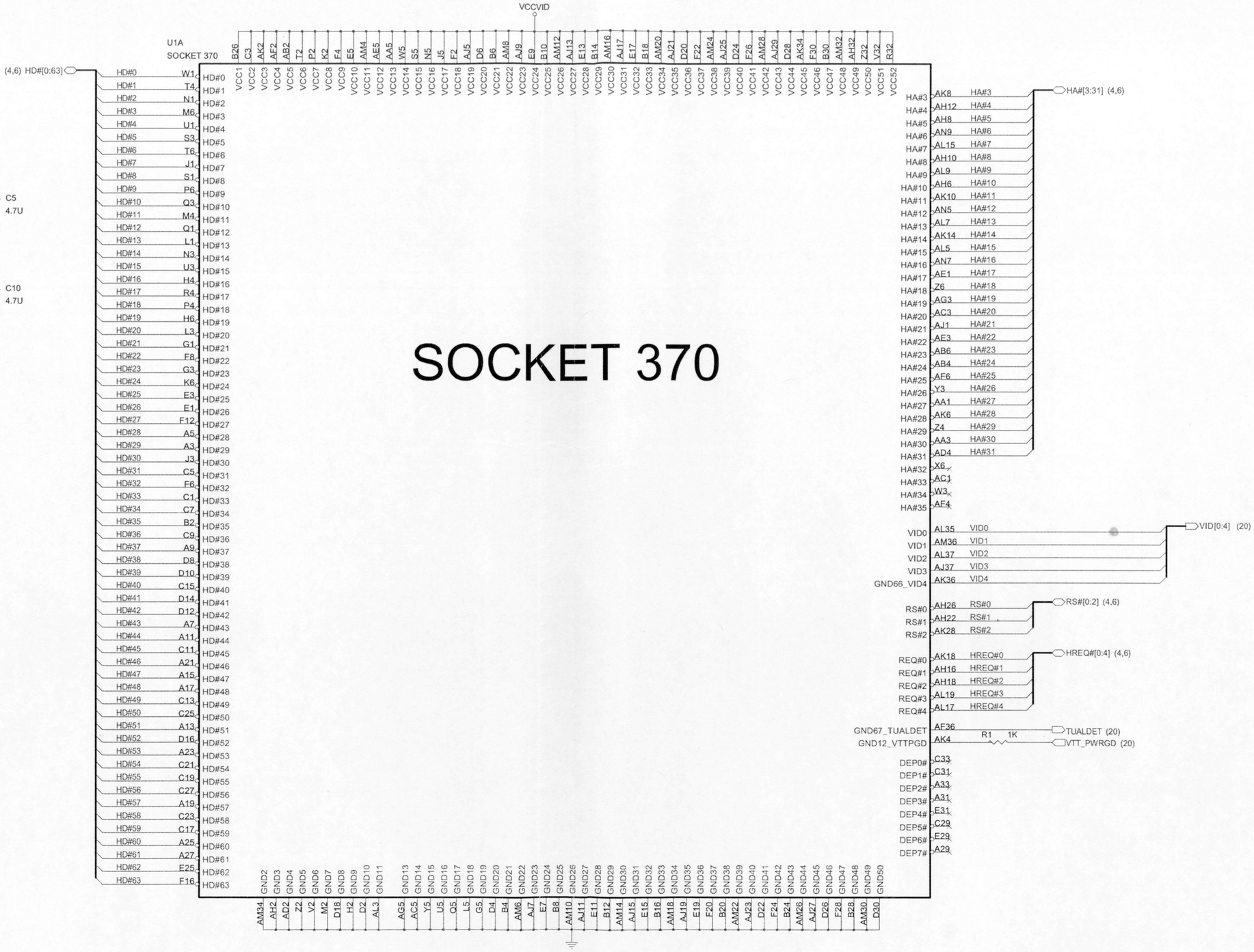
RTC- debe funcionar
BAT. para la fuente - VCMOS no sta en los esquemas
Posicionamiento de Socket 370
La señal VRM_PWRGD que sale del IRU3013 debe hacer la función de reset al bajar los 5Vcc por debajo de 4,70 Vcc ??
El modelo de conector no es AMP si no MOLEX (dos indicaron que no eran aceptados)
El conector del ventilador del pentium sera el standar de 3 pines CN9
Las distancias de socket 370 deben ser las standard para poner rodaderas standard
En el Gold Finger que lado sera el de componets y cual el de soldaduras
La salida VGA sera de 8 pins 3 de masa y R, G, B, HSYNC, VSYNC en tres de pines.
La señal CLKG_WDT porque esta conectada al diodo D1 del CLK Esquema 5

			EPoX COMPUTER CO., LTD		SCALE NONE	DRAWING DATE 2002-07-26	DRAWING TITLE D815E	Size A3	Description COVER SHEET	Rev. 0.0
			APPROVED MACRO	DESIGNED PING	DRAWN JOYCE	CUSTOMER NAME EPoX	JOB No. -	Sheet 1 of 21		

La 93C46-3.3V U11 del esquema 2.1 Es necesaria

SOCKET 370





			EPoX COMPUTER CO., LTD		SCALE	DRAWING DATE	DRAWING TITLE	Size	Description	Rev.
					NONE	2002-07-26	D815E	A3	SOCKET370 1/2	0.0
			APPROVED	DESIGNED	DRAWN	CUSTOMER NAME	JOB No.	Sheet 2 of 21		
			MACRO	PING	JOYCE	EPoX	-			

SOCKET 370

U1B
SOCKET 370

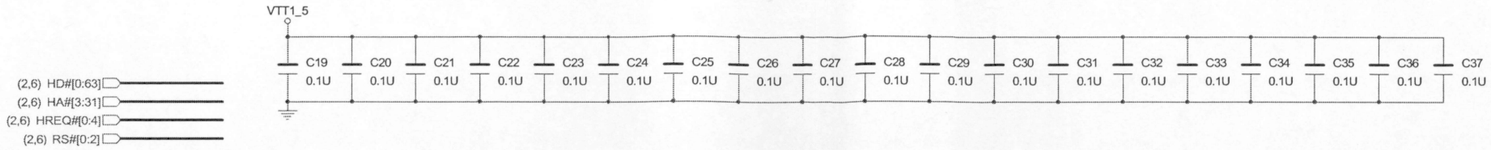
VTT1_5 R4 75.0 1% R5 150 1% C12 0.1U C13 0.1U C14 0.1U C15 0.1U
CPU_GTLREF
VCC2_5 (20) TUALDET5V# Q1 IRLML2803
VCMOS R2 75.0 1% R3 150 1% C11 0.1U
VCC5 JP1 PH205
CPU_TDI AN35 TDI
CPU_TDO AN37 TDO
CPU_TRST# AN33 TRST#
CPU_TCK AL33 TCK
CPU_TMS AK32 TMS
CPU_ITPREQ# J37 PREQ#
R9 330 R6 39 R10 150 R11 330 R12 680 R13 39 R14 330
A35 PRDY#
G33 BP2#
E37 BP3#
C35 BPM0#
E35 BPM1#
R22 14.0 1%
N33 RSRVD6
N35 RSRVD7
N37 RSRVD8
Q33 RSRVD9
Q35 RSRVD10
Q37 RSRVD11
R25 10K
AK30 RSRVD12
AM2 RSRVD13
F10 RSRVD29
W35 RSRVD45
Y1 RSRVD47
R2 RSRVD50
L33 RSRVD32
X2 RSRVD52
R26 150 APICD0 R30 150 APICD1 R27 86.6 1% R28 330 R29 @56
G37 VTT
APICD0 J35 PICD0
APICD1 L35 PICD1
(5) APICCLK_CPU J33 PICCLK
(5) CPUHCLK CPUHCLK W37 BCLK
CPU_CLKREF Y33 CLKREF
(12) CPU_PWRGD AK26 PWRGOOD
(6) CPURST# CPURST# AH4 RESET#
R35 1K X4 RESET2#
AG1 EDGCTRL
R32 150 1% R33 150 1% C16 4.7U
C37 CPUPRES#
R36 22 R37 1.8K
U37 VTT1_5A
U35 VTT1_5A
S37 VTT1_5A
S33 VTT1_5A
E23 VTT1_5A
AN21 VTT1_5A
AA35 VTT1_5A
AA33 VTT1_5A
C17 @18P C18 10P
(5,7,20) TUALDET5V Q2 IRLML2803
R41 51 R42 @1K VCCVID

AB36 V_CMOS
AD36 V1_5
Z36 V2_5
E33 VREF0
E18 VREF1
K4 VREF2
R6 VREF3
V6 VREF4
AD6 VREF5
AK12 VREF6
AK22 VREF7
M32 VCC53
H32 VCC54
AF34 VCC55
AB34 VCC56
X34 VCC57
T34 VCC58
P34 VCC59
K34 VCC60
F34 VCC61
B34 VCC62
AH36 VCC63
B22 VCC64
V36 VCC65
R36 VCC66
H36 VCC67
D36 VCC68
D32 VCC69
AD32 VCC70
AH24 VCC71
E14 VCC72
K32 VCC73
AA37 VCC74
Y35 VCC75
AN11 VTT1_5
AL21 VTT1_5
AL13 VTT1_5
AK16 VTT1_5
AH20 VTT1_5
AN15 VTT1_5
G35 VTT1_5

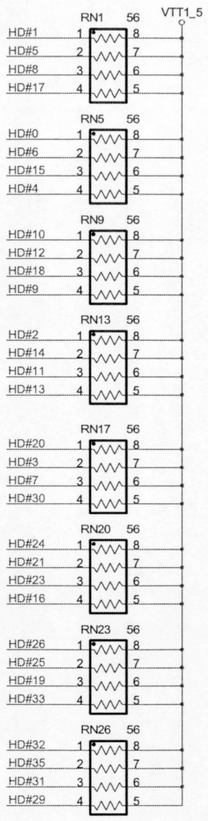
BNR# AH14 BNR# (4,6)
BPRI# AN17 BPRI# (4,6)
TRDY# AN25 HTRDY# (4,6)
DEFER# AN19 DEFER# (4,6)
LOCK# AK20 HLOCK# (4,6)
DRDY# AN27 DRDY# (4,6)
HITM# AL23 HITM# (4,6)
HIT# AL25 HIT# (4,6)
DBSY# AL27 DBSY# (4,6)
ADS# AN31 HADS# (4,6)
FLUSH# AE37 FLUSH R16 150 VCMOS
BSEL0# AJ33 BSEL0 (5,7)
BSEL1# AJ31 BSEL1 (5,7)
BR0# AN29 R20 33
THRMDP AL31
THRMDN AL29
THERMTRIP# AH28
A20M# AE33 A20M# (12)
STPCLK# AG35 STPCLK# (12)
SLP# AH30 CPUSLP# (12)
SMI# AJ35 SMI# (12)
LINT0/INTR M36 INTR (12)
LINT1/NMI L37 NMI (12)
INIT# AG33 INIT# (12,14)
FERR# AC35 FERR# FERR# (12)
IGNNE# AG37 IGNNE# (12)
IERR# AE35
PLL1 W33 L1 4.7UH R31 1 VCCVID
PLL2 U33 CS1 33U/8V
RSP# AC37
AP0# AL11 FERR# R34 150 VCMOS
AP1# AN13
RP# AN23
BINIT# B36
AERR# AK24
BERR# V4
SLEWCNTR E27 R38 110 1% R39 220
RTTCNTR S35
VCOREDET E21 VCOREDET (7) R40 121 1%

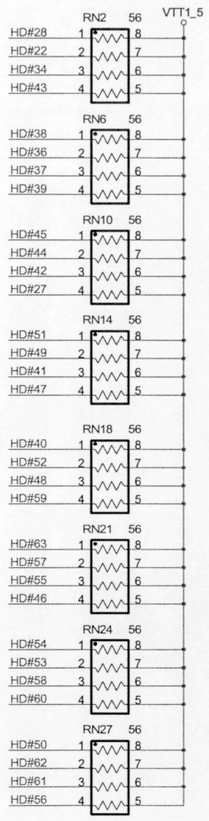
AE32 GND51
AB32 GND52
X32 GND53
T32 GND54
P32 GND55
E32 GND56
B32 GND57
AH34 GND58
AD34 GND59
Z34 GND60
V34 GND61
R34 GND62
M34 GND63
H34 GND64
D34 GND65
X36 GND68
T36 GND69
P36 GND70
K36 GND71
F36 GND72
A37 GND73
AC33 GND74
AJ3 GND75
AL1 GND76
AN3 GND77
Y37 GND78
CPURST# R43 1K R44 1K VTT1_5

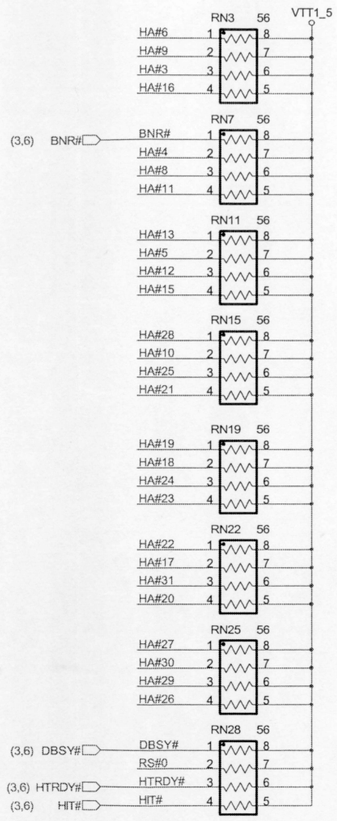
EPoX COMPUTER CO., LTD			SCALE NONE	DRAWING DATE 2002-07-26	DRAWING TITLE D815E	Size A3	Description SOCKET370 2/2	Rev. 0.0
APPROVED MACRO	DESIGNED PING	DRAWN JOYCE	CUSTOMER NAME EPoX		JOB No. -	Sheet 3 of 21		

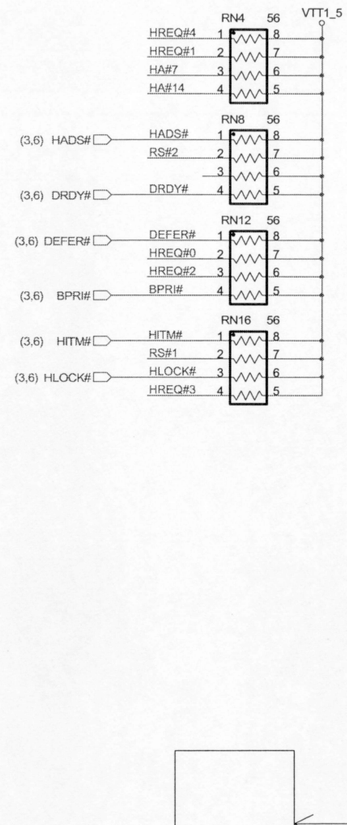


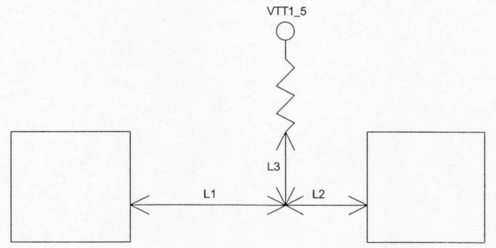
(2,6) HD#[0:63]
(2,6) HA#[3:31]
(2,6) HREQ#[0:4]
(2,6) RS#[0:2]







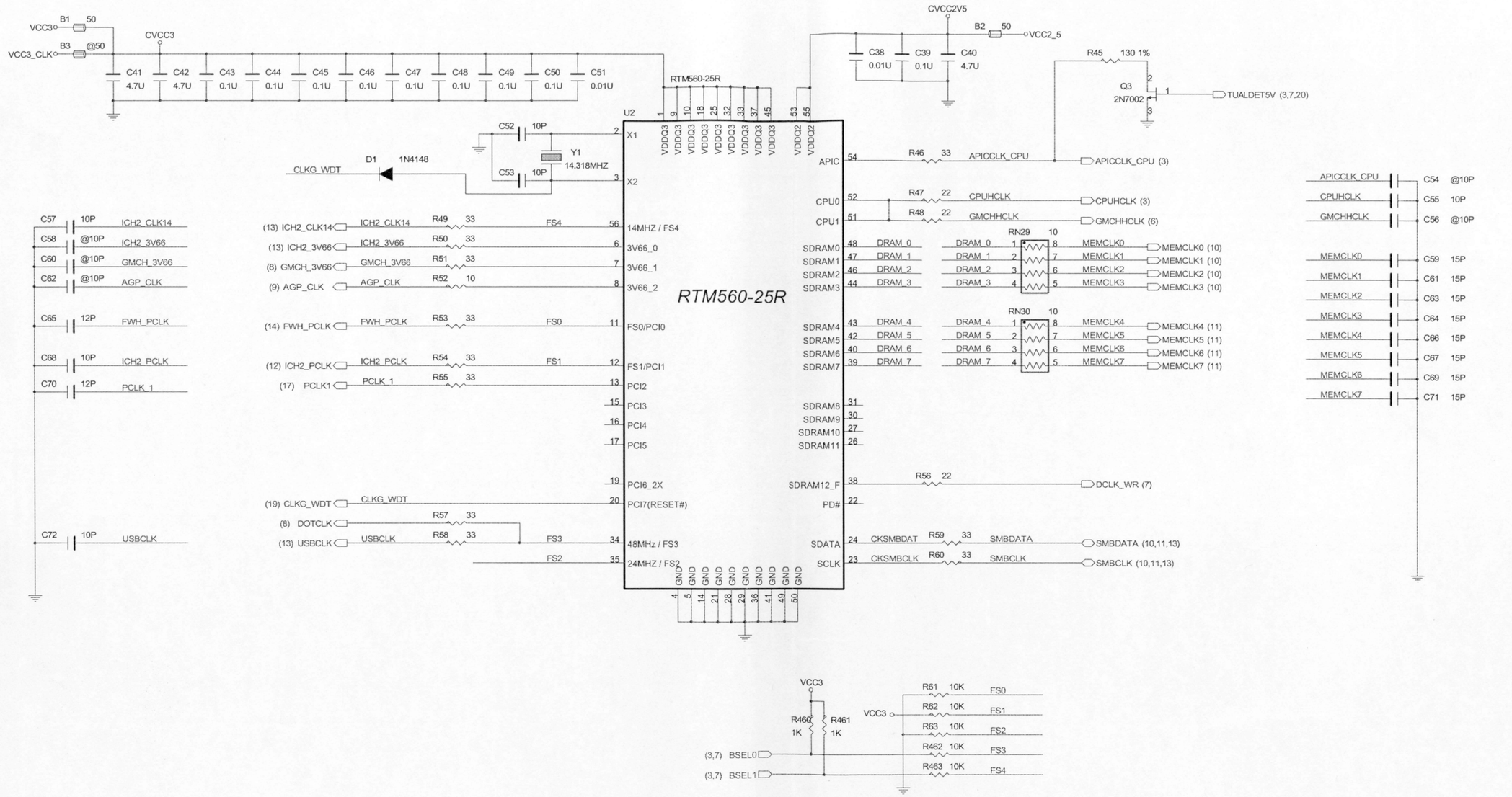




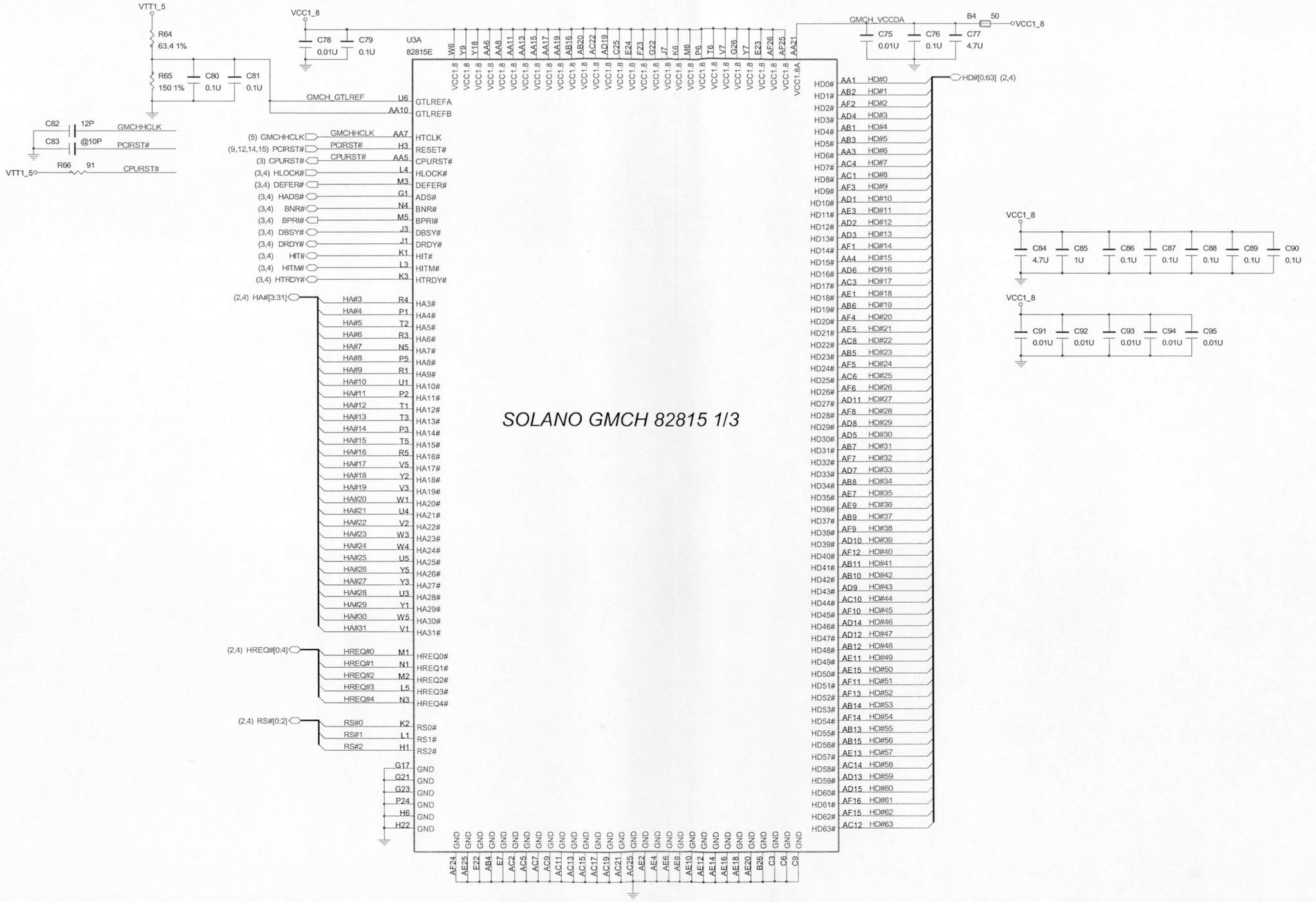
	Min.(inch)	Max.(inch)
L1	1.90	4.50
L2	0	0
L3	0.50	2.50

	Trace Width : Space Ratio (mil)
GTL Same group	5:10
GTL Different group	5:15
GTL to DIMM Group	5:30
GTL to non-GTL	5:20

			EPoX COMPUTER CO., LTD	SCALE NONE	DRAWING DATE 2002-07-26	DRAWING TITLE D815E	Size A3	Description GTL RESISTER	Rev. 0.0
			APPROVED MACRO	DESIGNED PING	DRAWN JOYCE	CUSTOMER NAME EPoX	JOB No. -	Sheet 4 of 21	

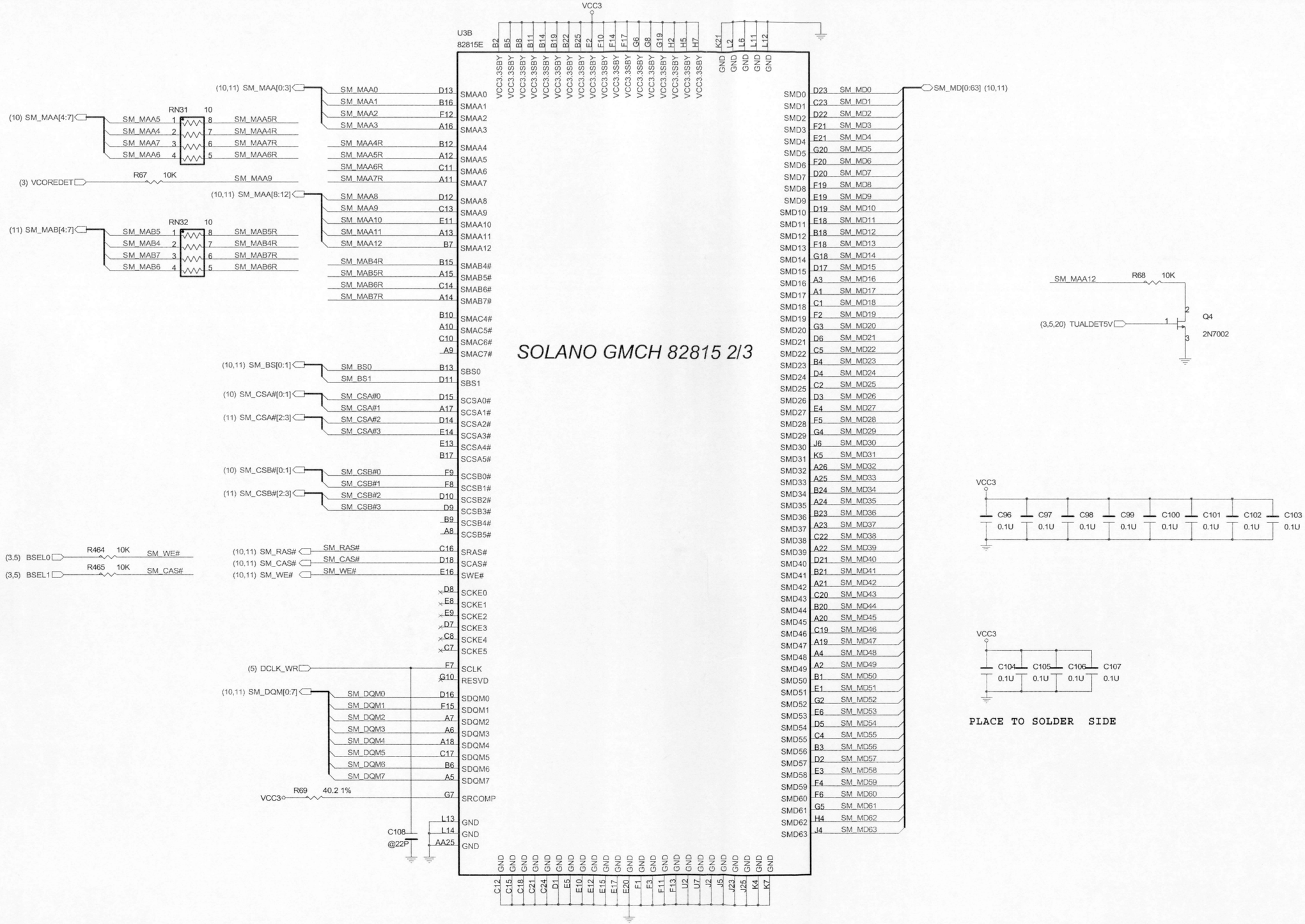


			EPoX COMPUTER CO., LTD		SCALE	DRAWING DATE	DRAWING TITLE	Size	Description / Rev.
					NONE	2002-07-26	D815E	A3	CLOCK SYNTESIZER / 0.0
			APPROVED	DESIGNED	DRAWN	CUSTOMER NAME	JOB No.	Sheet	
			MACRO	PING	JOYCE	EPoX	-	5	of 21



SOLANO GMCH 82815 1/3

			EPoX COMPUTER CO., LTD	SCALE	DRAWING DATE	DRAWING TITLE	Size	Description	Rev.
				NONE	2002-07-26	D815E	A3	GMCH_82815E 1/3	0.0
			APPROVED	DESIGNED	DRAWN	CUSTOMER NAME	JOB No.	Sheet 6 of 21	
			MACRO	PING	JOYCE	EPoX	-		



			EPoX COMPUTER CO., LTD	SCALE	DRAWING DATE	DRAWING TITLE	Size	Description	Rev.
				NONE	2002-07-26	D815E	A3	GMCH_82815E 2/3	0.0
			APPROVED	DESIGNED	DRAWN	CUSTOMER NAME	JOB No.	Sheet 7 of 21	
			MACRO	PING	JOYCE	EPoX	-		

SOLANO GMCH 82815 3/3

U3C
82815E

VDDQ
R70 301 1%
R71 200 1%
(9,19) TYPEDET#
Q5 2N7002
CAPGREF

(9) GAD[0:31]
GAD0 K26 GAD0/LDQM0
GAD1 J22 GAD1/LMD4
GAD2 K25 GAD2/LMD7
GAD3 J21 GAD3/LMD3
GAD4 L24 GAD4/LMD6
GAD5 J20 GAD5/LMD2
GAD6 L26 GAD6/LMD5
GAD7 K23 GAD7/LMD1
GAD8 K22 GAD8/LMD0
GAD9 M25 GAD9/LMA4
GAD10 M24 GAD10/LDQM1
GAD11 M26 GAD11/LMA2
GAD12 M21 GAD12/LMD8
GAD13 N24 GAD13/LMA5
GAD14 N22 GAD14/LMD9
GAD15 N26 GAD15/LMA1
GAD16 T26 GAD16/LMA8
GAD17 T22 GAD17/LMD14
GAD18 U24 GAD18/LMA11
GAD19 T23 GAD19/LMD15
GAD20 U26 GAD20/LMA9
GAD21 T24 GAD21/LMD16
GAD22 V24 GAD22/LCS#
GAD23 U21 GAD23/LMD17
GAD24 V25 GAD24/LCKE
GAD25 V21 GAD25/LMD18
GAD26 V26 GAD26/LCAS#
GAD27 W21 GAD27/LMD19
GAD28 W24 GAD28/LTCK1
GAD29 W22 GAD29/LMD20
GAD30 W26 GAD30/LTCK0
GAD31 Y21 GAD31/LMD21

(9) GCBE#[0:3]
GCBE#0 H23 GCBE#0/LMA3
GCBE#1 N21 GCBE#1/LMD11
GCBE#2 T25 GCBE#2/LMD13
GCBE#3 Y26 GCBE#3/LRAS#

(9) GFRAME# GFRAME# R26 GFRAME#/LMA10
(9) GDEVSEL# GDEVSEL# P26 GDEVSEL#/LMD11
(9) GIRDY# GIRDY# P23 GIRDY#/LMD12
(9) GTRDY# GTRDY# P21 GTRDY#/LMA7
(9) GSTOP# GSTOP# P25 GSTOP#/LMA0
(9) GPAR GPAR# R24 GPAR#/LMA6
(9) GREQ# GREQ# AE26 GREQ#/LMD27
(9) GGNT# GGNT# AD25 GGNT#
(9) PIPE# PIPE# AC26 PIPE#/LMD24

(9) ADSTB0 ADSTB0 M22 ADSTB0
(9) ADSTB0# ADSTB0# L23 ADSTB0#
(9) ADSTB1 ADSTB1 U22 ADSTB1
(9) ADSTB1# ADSTB1# V23 ADSTB1#
(9) SBSTB SBSTB Y23 SBSTB
(9) SBSTB# SBSTB# AA24 SBSTB#

(9) ST[0:2]
ST0 AD24 ST0/LMD28
ST1 AC24 ST1/LDQM3
ST2 AC23 ST2/LMD29

(9) RBF# RBF# AD26 RBF#/LMD30
(9) WBF# WBF# AB24 WBF#

(9) CAGPREF CAPGREF J24 AGPREF
R103 40.2 1% J26 GRCOMP
R104 10.0 1% OCLK R22 LOCLK
RCLK P22 LRCLK
R105 @8.2K
C124 22P

VCC3
RN33 8.2K
4 5 GTRDY#
3 6 GDEVSEL#
2 7 GIRDY#
1 8 GFRAME#
RN34 8.2K
1 8 GGNT#
2 7 GREQ#
3 6 GSTOP#
4 5
R88 8.2K PIPE#
R89 8.2K RBF#
R91 8.2K ADSTB0
R92 8.2K ADSTB1
R93 8.2K WBF#
R94 8.2K SBSTB
R95 8.2K ST0
R97 8.2K ST1
R98 8.2K ST2
R99 8.2K GPAR#
R100 8.2K ADSTB0#
R101 8.2K ADSTB1#
R102 8.2K SBSTB#
C123 0.1U CAPGREF

LTVDATA0 AD16
LTVDATA1 AE17
LTVDATA2 AE17
LTVDATA3 AD17
LTVDATA4 AE18
LTVDATA5 AD18
LTVDATA6 AF20
LTVDATA7 AD20
LTVDATA8 AC20
LTVDATA9 AF21
LTVDATA10 AE21
LTVDATA11 AD21
LTVBLANK# AB19
TVCLKIN/SL_STALL AC18 R72 8.2K VCC3
LTVCLKOUT0 AE19
LTVCLKOUT1 AF19
TVVSYNC AC16
TVHSYNC AB17
LTVDA AB21 R75 8.2K VCC3
LTVCL AA20 R76 8.2K VCC3
VCC3 VCC3
R73 @8.2K R74 @8.2K
DDCCK AB18 R77 0 VGA_DDCCL (18)
DDCDA AA18 R78 0 VGA_DDCDA (18)
DCLKREF AE24 R79 0 DOTCLK (5)
IWASTE Y20
IREF AD23 RSET R80 @8.2K
C119 18P
R81 174 1%
VSYNC AF22 R82 0 VGA_VSYNC (18)
HSYNC AF23 R83 0 VGA_HSYNC (18)
RED AD22 R84 0 VGA_RED (18)
GREEN AE22 R85 0 VGA_GREEN (18)
BLUE AE23 R86 0 VGA_BLUE (18)
HLCLK F22 GMCH_3V66 GMCH_3V66 (5)
HL0 H24 HL0
HL1 H26 HL1
HL2 H25 HL2
HL3 G24 HL3
HL4 F24 HL4
HL5 E26 HL5
HL6 E25 HL6
HL7 D26 HL7
HL8 D25 HL8
HL9 D24 HL9
HL10 C26 HL10 HL[0:10] (12)
HUBREF H21 GMCH_HUBREF
HLSTRB G25 HLSTB HLSTB (12)
HLSTRB# F26 HLSTB# HLSTB# (12)
HLZCOMP H20 R96 40.2 1% VCC1_8
SBA0/LMD31 AB22 SBA0
SBA1/LMD25 AB25 SBA1
SBA2/LDQM2 AB23 SBA2
SBA3/LMD26 AB26 SBA3
SBA4/LMD23 AA22 SBA4
SBA5/WE# AA26 SBA5
SBA6/LMD22 Y22 SBA6
SBA7/LGM_FREQ_SEL Y25 SBA7
SBA[0:7] (9)
GMCH_3V66 C120 22P
VCC1_8
R87 301 1%
C121 0.01U C122 0.1U R90 301 1%

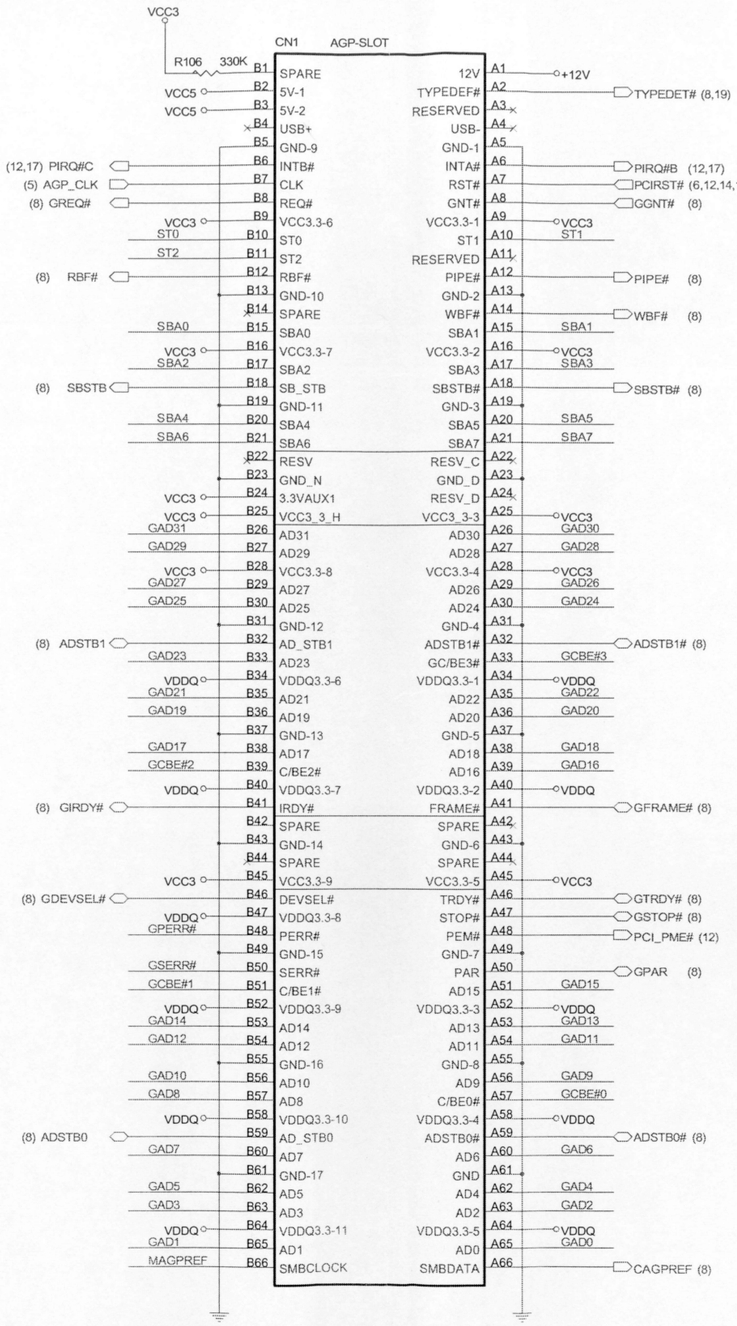
GND N16 N23 P4 AA23 F16 F25 G9
GND P16 R2 R6 R11 R12 R13 R14 R15 R16 R23 R25 T4 T11 T12 T13 T14 T15 T16 L15 L16 L22 L25 M4 M11 M12 M13 M14 M15 M16 N2 N6 N11 N12 N13 N14 N15

VDDQ
C109 0.1U C110 0.1U C111 0.1U C112 0.1U C113 0.1U C114 0.1U C115 0.1U
VDDQ
C116 @0.1U C117 @0.1U C118 @0.1U

19+5
24

		EPoX COMPUTER CO., LTD	SCALE NONE	DRAWING DATE 2002-07-26	DRAWING TITLE D815E	Size A3	Description GMCH_82815E 3/3	Rev. 0.0
		APPROVED MACRO	DESIGNED PING	DRAWN JOYCE	CUSTOMER NAME EPoX	JOB No. -	Sheet 8 of 21	

(8) GAD[0:31]
(8) GCBE#[0:3]
(8) ST[0:2]
(8) SBA[0:7]

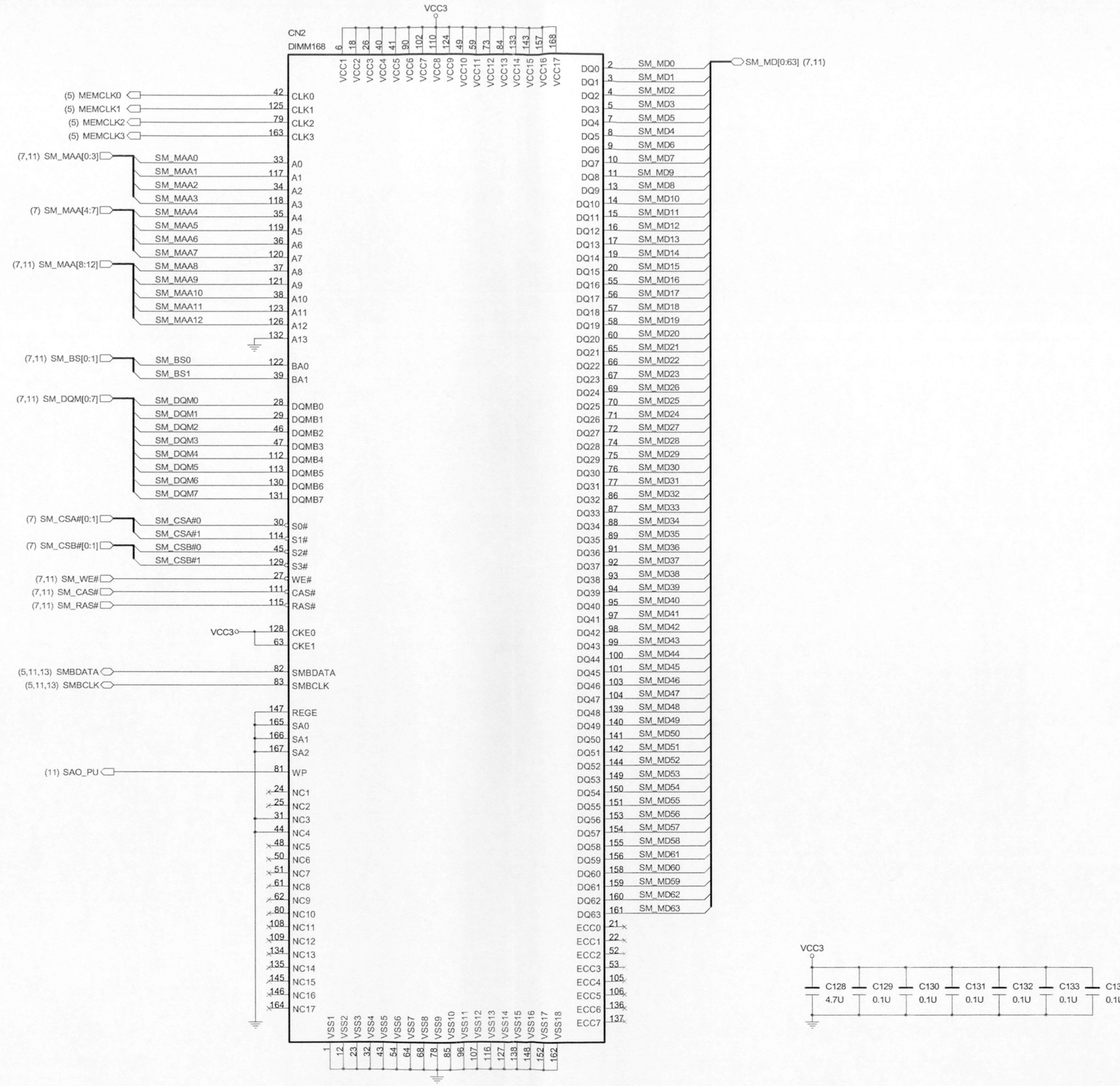


VDDQ
CE1 6MV1000CA
CE2 6MV1000CA

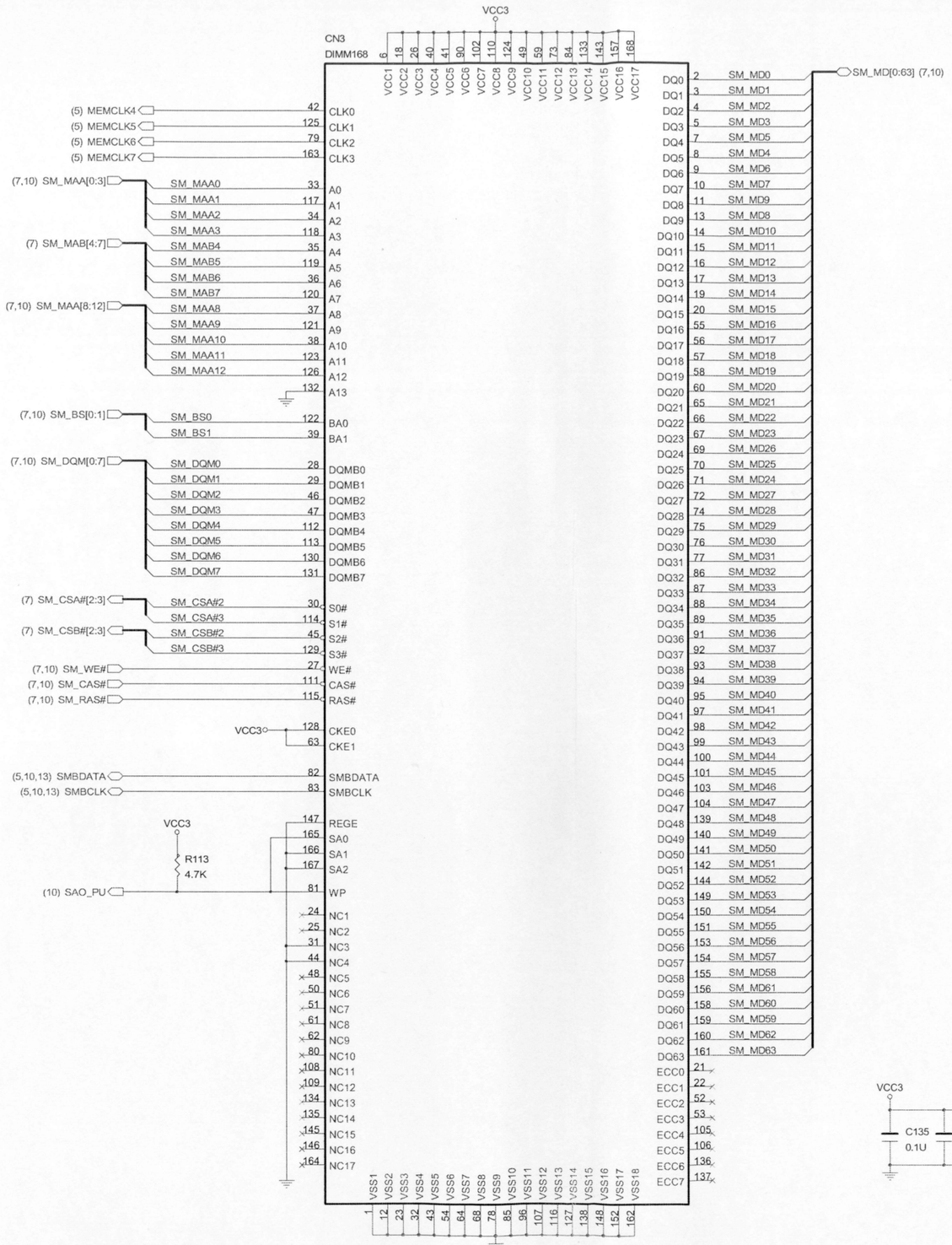
VCC3
R107 8.2K GPERR#
R108 8.2K GSERR#

VDDQ
C125 470P
R109 82
R110 1K
MAGPREF
R111 82
R112 1.5K
C126 0.1U
C127 470P

			EPoX COMPUTER CO., LTD	SCALE NONE	DRAWING DATE 2002-07-26	DRAWING TITLE D815E	Size A3	Description AGP SLOT	Rev. 0.0
			APPROVED MACRO	DESIGNED PING	DRAWN JOYCE	CUSTOMER NAME EPoX	JOB No. -	Sheet 9 of 21	



	EPoX COMPUTER CO., LTD		SCALE: NONE	DRAWING DATE: 2002-07-26	DRAWING TITLE: D815E	Size: A3	Description: DIMM 1/2	Rev.: 0.0
	APPROVED: MACRO	DESIGNED: PING	DRAWN: JOYCE	CUSTOMER NAME: EPoX	JOB No.: -	Sheet 10 of 21		



			EPoX COMPUTER CO., LTD		SCALE	DRAWING DATE	DRAWING TITLE	Size	Description	Rev.
					NONE	2002-07-26	D815E	A3	DIMM 2/2	0.0
			APPROVED	DESIGNED	DRAWN	CUSTOMER NAME	JOB No.	Sheet		
			MACRO	PING	JOYCE	EPoX	-	11	of	21

ICH2 82801BA

U4B
82801BA

RN35 2.7K
PIRQ#D 1
PIRQ#C 2
PIRQ#B 3
PIRQ#A 4
8 7 6 5

RN36 2.7K
DEVSEL# 1
TRDY# 2
IRDY# 3
FRAME# 4
8 7 6 5

RN37 2.7K
SERR# 1
PERR# 2
PLOCK# 3
STOP# 4
8 7 6 5

RN38 5.6K
PREQ#1 1
2
PREQ#2 3
PREQ#4 4
8 7 6 5

RN39 2.7K
PREQ#0 1
PGNT#2 2
PGNT#0 3
PGNT#1 4
8 7 6 5

PGNT#4 R128 5.6K
PGNT#5 R129 5.6K
PCPCI_GNT#A R130 8.2K
PCPCI_REQ#A R131 8.2K

C143 @10P DEVSEL#
C144 47P PCIRST#

GPIO2 R134 4.7K
GPIO3 R135 4.7K
GPIO4 R136 4.7K
GPIO5 R137 4.7K
GPIO6 R138 8.2K
R139 @1K
GPIO7 R140 8.2K
GPIO12 R141 8.2K
GPIO13 R142 8.2K
R143 470
GPIO18 R144 @8.2K
GPIO19 R145 @8.2K
GPIO20 R146 @8.2K
GPIO23 R147 @8.2K
LPC_PME# R148 8.2K
FWH_WP# R149 8.2K
GPIO25 R150 8.2K
GPIO27 R151 8.2K
GPIO28 R152 8.2K

PREQ#3 R117 5.6K
PREQ#5 R120 5.6K
PGNT#3 R123 5.6K

(17) AD[31:0]
(17) C_BE#[0:3]
(17) DEVSEL#
(17) FRAME#
(17) IRDY#
(17) TRDY#
(17) STOP#
(17) PAR
(6,9,14,15) PCIRST#
(17) PLOCK#
(17) SERR#
(17) PERR#
(9) PCI_PME#
(5) ICH2_PCLK
(14) FWH_WP#
(17) GPIO25
(17) GPIO27
(17) GPIO28

AD0	AA4	AD1	AB4
AD2	Y4	AD3	W5
AD4	W4	AD5	Y5
AD6	AB3	AD7	AA5
AD8	AB5	AD9	Y3
AD10	W6	AD11	W3
AD12	Y6	AD13	Y2
AD14	AA6	AD15	Y1
AD16	V2	AD17	AA8
AD18	V1	AD19	AB8
AD20	U4	AD21	W9
AD22	U3	AD23	Y9
AD24	U2	AD25	AB9
AD26	U1	AD27	W10
AD28	T4	AD29	Y10
AD30	T3	AD31	AA10
C_BE#0	AA3	C_BE#1	AB6
C_BE#2	Y8	C_BE#3	AA9
DEVSEL#	AB7	FRAME#	V3
IRDY#	W8	TRDY#	V4
STOP#	W1	PAR	W2
PCIRST#	AA15	PLOCK#	AA7
SERR#	W7	PERR#	Y7
PME#	Y15	REQA#/GPIO0	M3
GNTA/GPIO16	L2	PCICLK	W11
PIRQE#/GPIO2	N3	PIRQF#/GPIO3	N2
PIRQG#/GPIO4	N1	PIRQH#/GPIO5	M4
GPIO6	Y11	GPIO7	AA11
GPIO8	Y14	GPIO12	W14
GPIO13	AB15	GPIO18	A15
GPIO19	D14	GPIO20	C14
GPIO21	L1	GPIO22	B14
GPIO23	A14	GPIO24	V21
GPIO25	W15	GPIO27	AB14
GPIO28	AA14		

A20M# D11 A20M# (3)
CPUSLP# A12 CPUSLP# (3)
FERR# R22 FERR# (3)
IGNNE# A11 IGNNE# (3)
INIT# C12 INIT# (3,14)
INTR C11 INTR (3)
NMI B11 NMI (3)
SMI# B12 SMI# (3)
STPCLK# C10 STPCLK# (3)
RCIN# B13 RCIN#
A20GATE C13 A20GATE
CPUPWRGD A13 CPU_PWRGD (3)

HL0 A4 HL0
HL1 B5 HL1
HL2 A5 HL2
HL3 B6 HL3
HL4 B7 HL4
HL5 A8 HL5
HL6 B8 HL6
HL7 A9 HL7
HL8 C8 HL8
HL9 C6 HL9
HL10 C7 HL10
HL11 C5 HL11
HL[0:10] (8)

R124 @0

HL_STB A6 HLSTB (8)
HL_STB# A7 HLSTB# (8)
HLCOMP A3 ICHCOMP_PU
HUBREF B4 ICH_HUBREF
R126 40.2 1%
VCC1_8

PIRQA# P1 PIRQ#A PIRQ#A (17)
PIRQB# P2 PIRQ#B PIRQ#B (9,17)
PIRQC# P3 PIRQ#C PIRQ#C (9,17)
PIRQD# N4 PIRQ#D PIRQ#D (17)

IRQ14 F21 IRQ14 IRQ14 (15)
IRQ15 C16 IRQ15
APICLK N20
APICD0 P22
APICD1 N19
SERIRQ N21 SERIRQ
R132 10K
R133 10K

REQ0# R2 PREQ#0 PREQ#0 (17)
REQ1# R3 PREQ#1
REQ2# T1 PREQ#2
REQ3# AB10 PREQ#3
REQ4# P4 PREQ#4
REQ5#/REQB#/GPIO1 L3 PREQ#5

GNT0# M2 PGNT#0 PGNT#0 (17)
GNT1# M1 PGNT#1
GNT2# R4 PGNT#2
GNT3# T2 PGNT#3
GNT4# R1 PGNT#4
GNT5#/GNTB#/GPIO17 L4 PGNT#5

LAN_RXD0 G2 LAN_RXD0 (21)
LAN_RXD1 G1 LAN_RXD1 (21)
LAN_RXD2 H1 LAN_RXD2 (21)
LAN_TXD0 F3 LAN_TXD0 (21)
LAN_TXD1 F2 LAN_TXD1 (21)
LAN_TXD2 F1 LAN_TXD2 (21)
LAN_CLK G3 LAN_CLK (21)
LAN_RSTSYNC H2 LAN_RSTSYNC (21)

GND D7
GND D8
GND D9
GND E6
GND E7

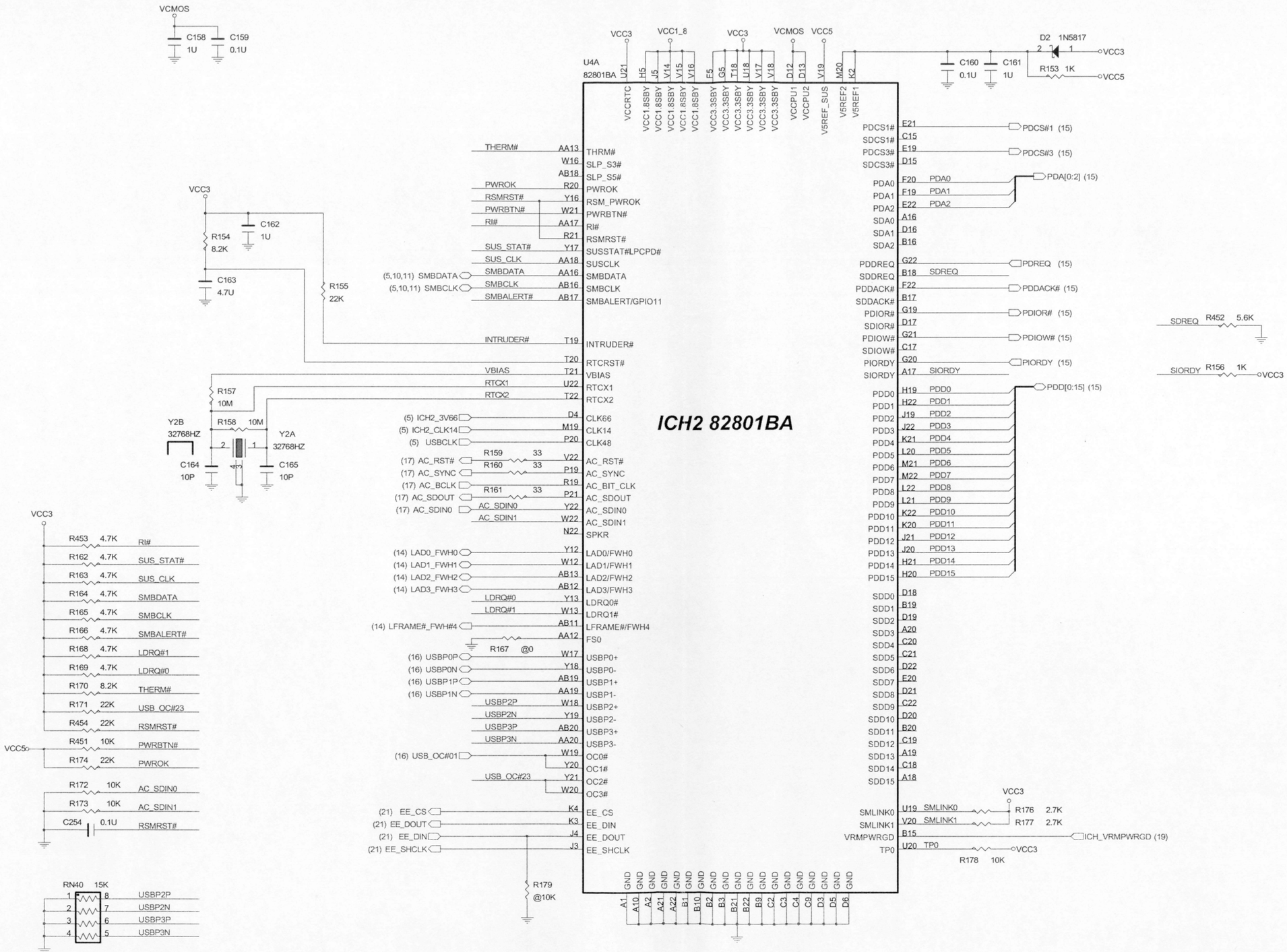
VCMOS
R114 330
R115 33
C141 @10P

RCIN# R116 8.2K
A20GATE R118 8.2K
IRQ14 R119 8.2K
IRQ15 R121 8.2K
SERIRQ R122 8.2K

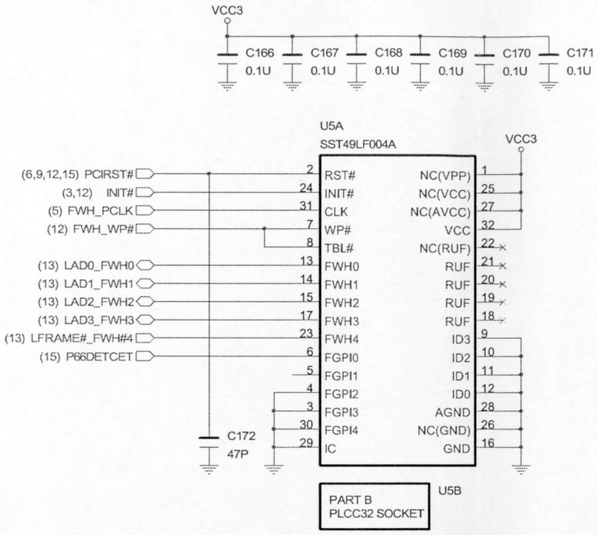
VCC1_8
R125 301 1%
R127 301 1%
C142 0.1U

VCC1_8: C145 0.1U, C146 0.1U, C147 0.1U, C148 0.1U
VCC3: C149 0.1U, C150 0.1U, C151 0.1U, C152 0.1U, C153 0.1U
VCC3: C154 0.1U, C155 0.1U, C156 0.1U, C157 0.1U

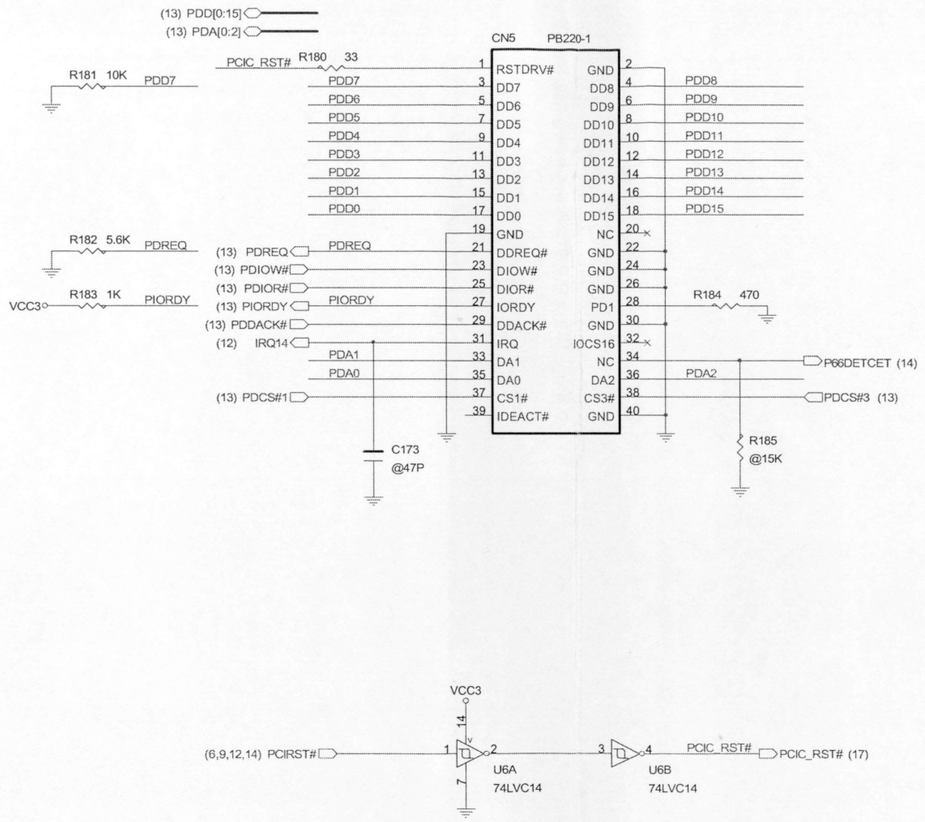
EPoX COMPUTER CO., LTD			SCALE NONE	DRAWING DATE 2002-07-26	DRAWING TITLE D815E	Size A3	Description ICH2_82801BA 1/2	Rev. 0.0
APPROVED MACRO	DESIGNED PING	DRAWN JOYCE	CUSTOMER NAME EPoX		JOB No. -	Sheet 12 of 21		



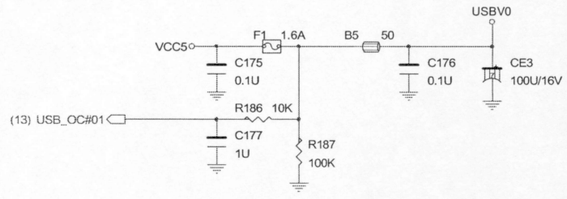
		EPoX COMPUTER CO., LTD			SCALE NONE	DRAWING DATE 2002-07-26	DRAWING TITLE D815E	Size A3	Description ICH2_82801BA 2/2	Rev. 0.0
		APPROVED MACRO	DESIGNED PING	DRAWN JOYCE	CUSTOMER NAME EPoX		JOB No. -	Sheet 13 of 21		

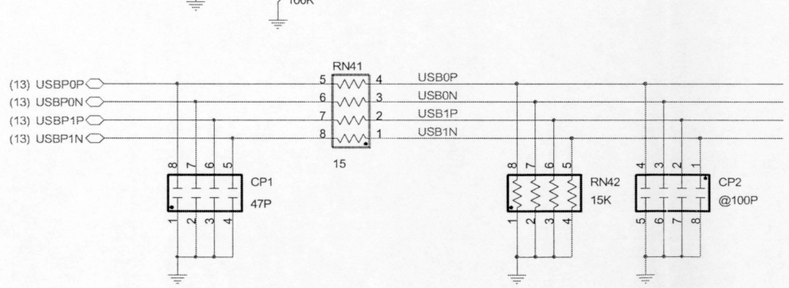


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△										
△			APPROVED MACRO	DESIGNED PING	DRAWN JOYCE	CUSTOMER NAME EPoX	JOB No. -	Sheet 14 of 21		
△										

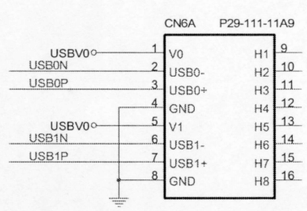


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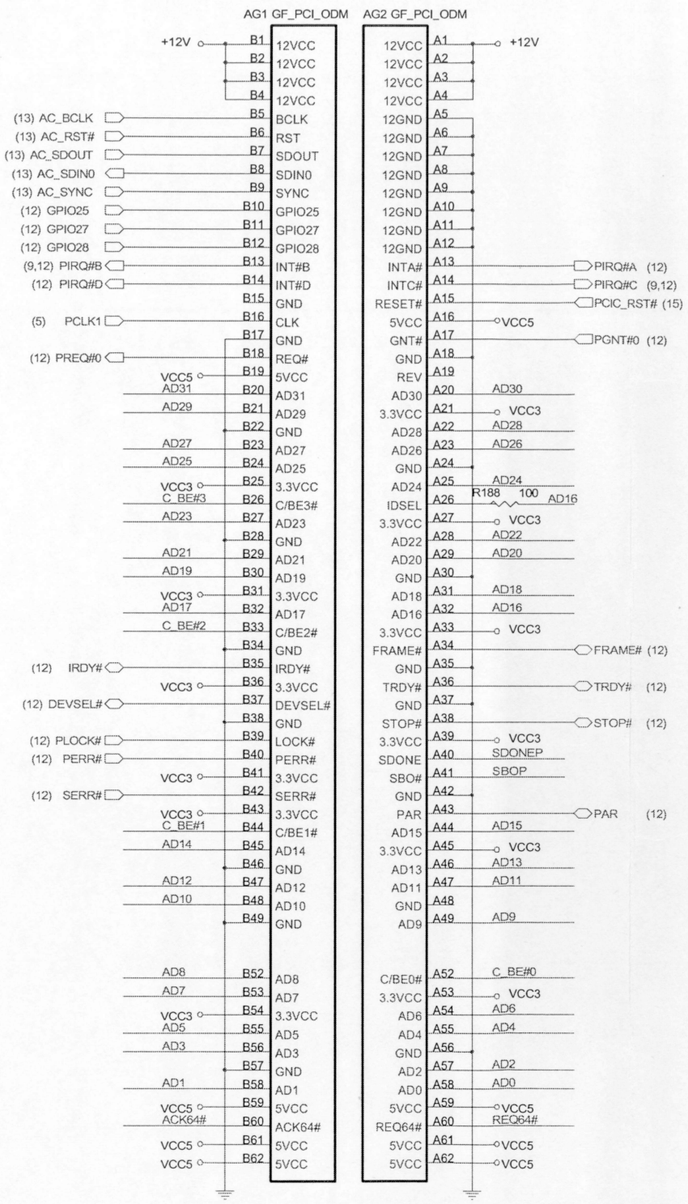


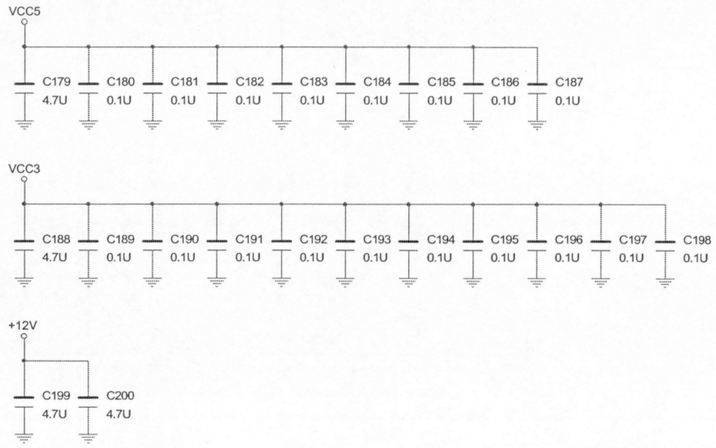
USB PORT

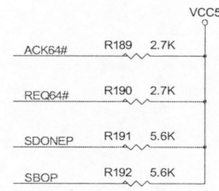


△			EPoX COMPUTER CO., LTD	SCALE NONE	DRAWING DATE 2002-07-26	DRAWING TITLE D815E	Size A3	Description USB PORT	Rev. 0.0
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△			APPROVED MACRO	DESIGNED PING	DRAWN JOYCE	CUSTOMER NAME EPoX	JOB No. -	Sheet 16 of 21	
△									

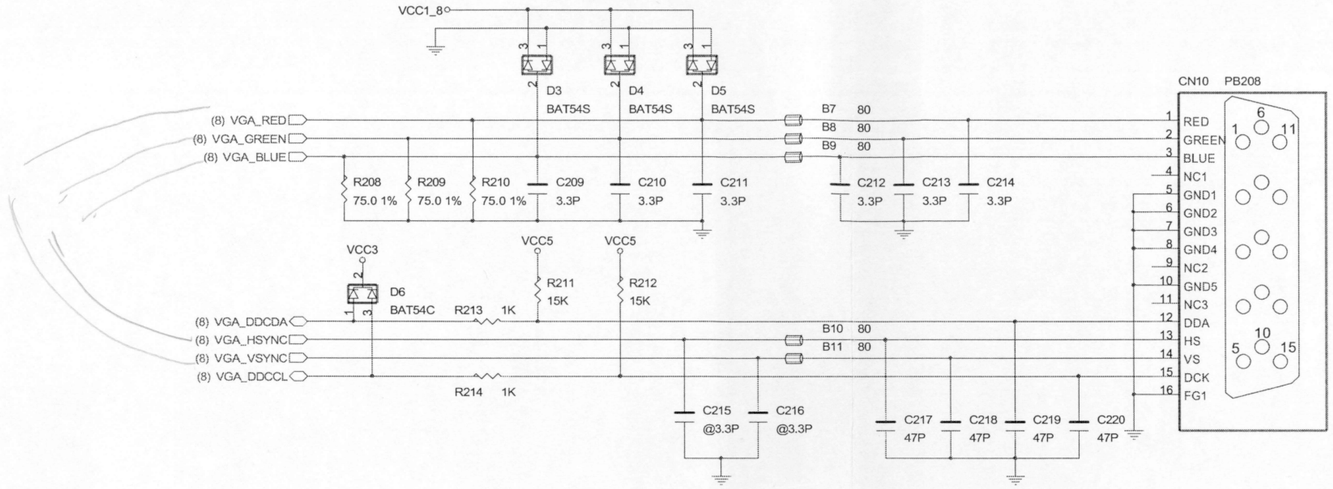
(12) AD[0:31]
(12) C_BE#[0:3]



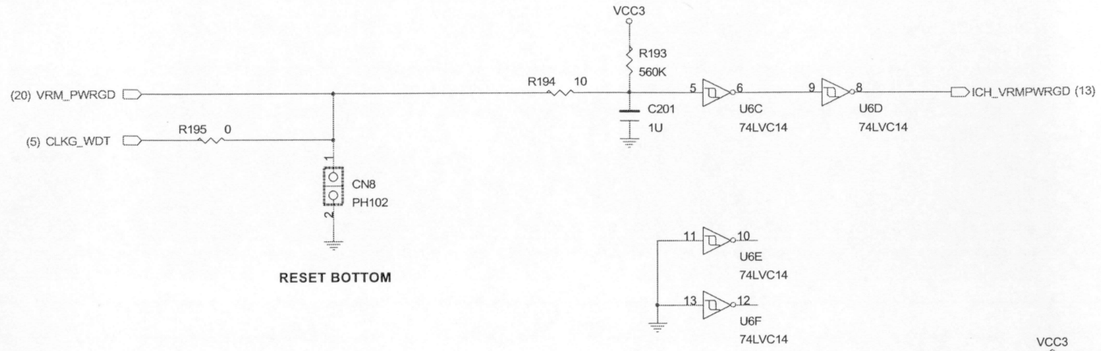


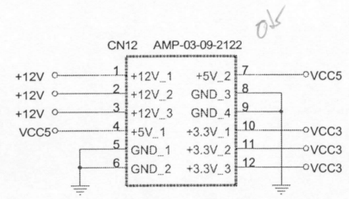


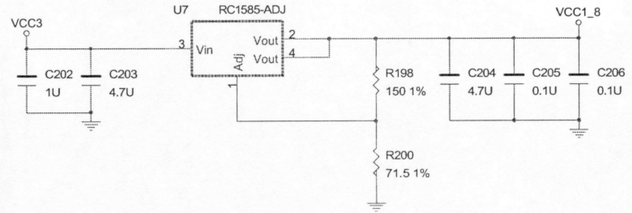
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			APPROVED MACRO	DESIGNED PING	DRAWN JOYCE	CUSTOMER NAME EPoX	JOB No. -	Sheet 17 of 21		

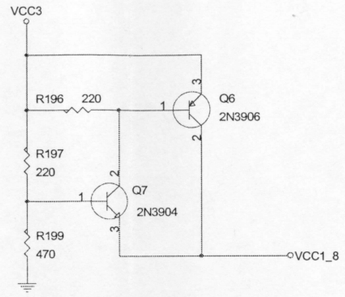


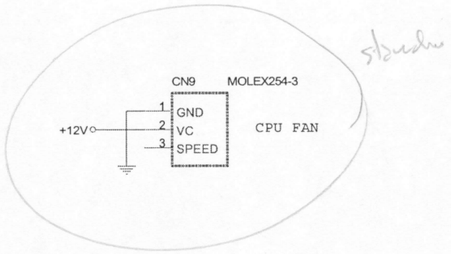
△			EPoX COMPUTER CO., LTD			SCALE NONE	DRAWING DATE 2002-07-26	DRAWING TITLE D815E	Size A3	Description VGA CONNECTOR	Rev. 0.0
△										
△			APPROVED MACRO	DESIGNED PING	DRAWN JOYCE	CUSTOMER NAME EPoX		JOB No. -	Sheet 18 of 21	
△										

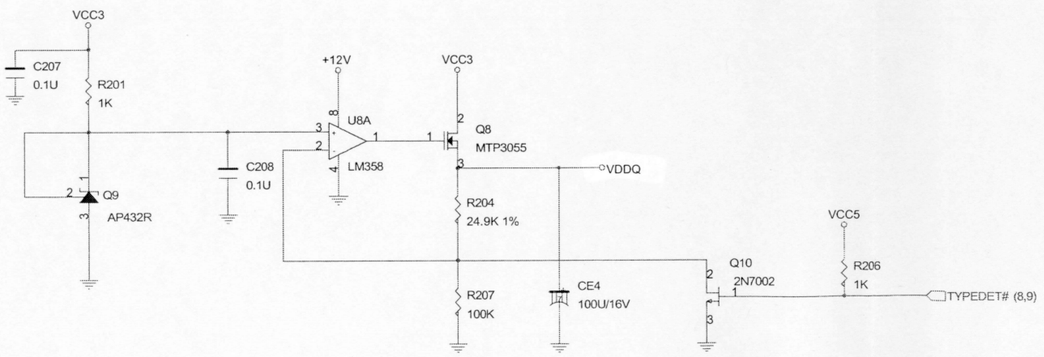


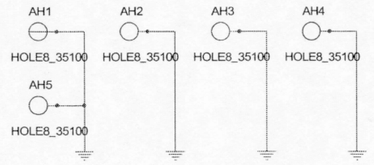






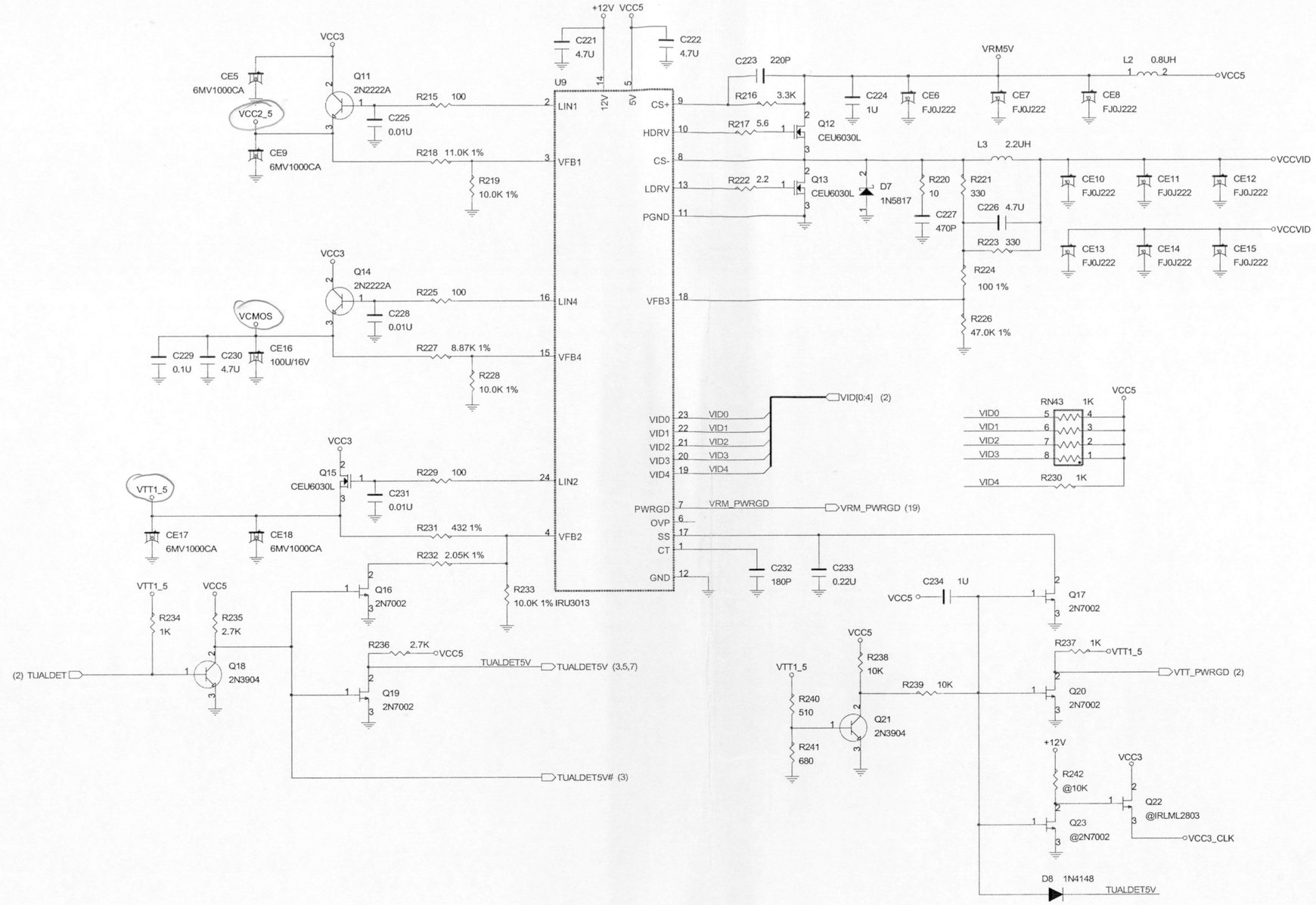




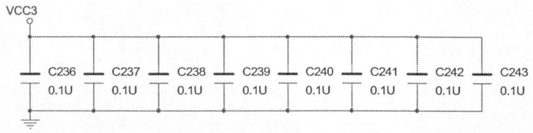


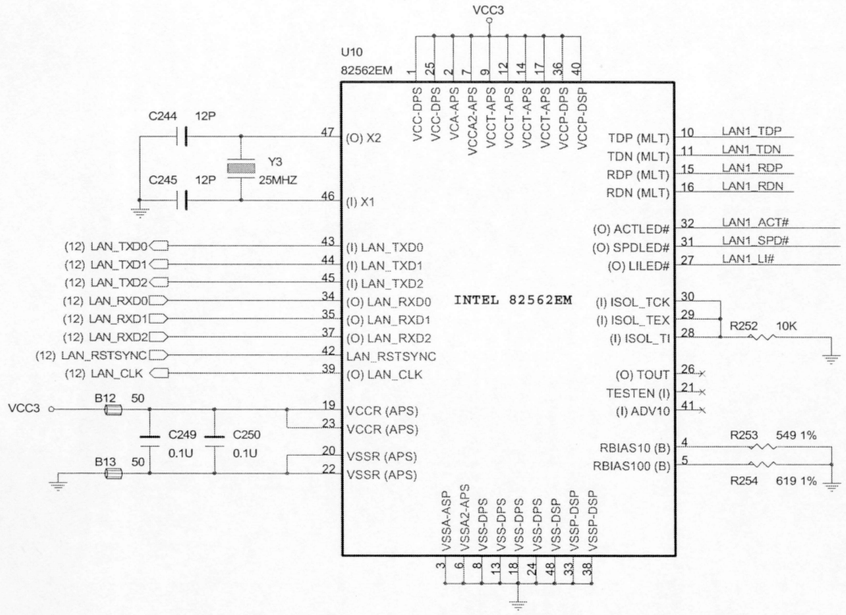


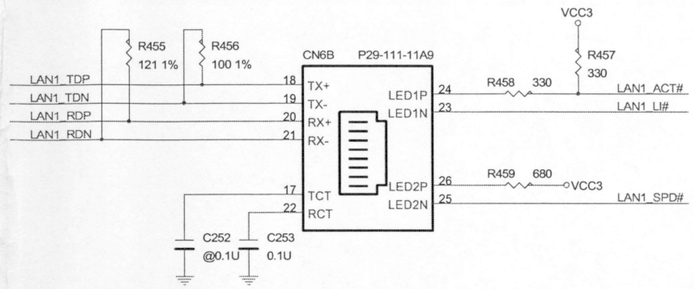
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		APPROVED: MACRO / DESIGNED: PING / DRAWN: JOYCE	CUSTOMER NAME: EPoX		JOB No.: -	Sheet 19 of 21		

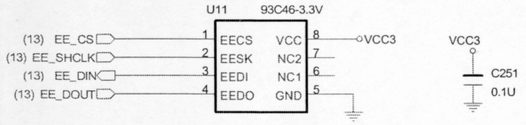


			EPoX COMPUTER CO., LTD		SCALE NONE	DRAWING DATE 2002-07-26	DRAWING TITLE D815E	Size A3	Description VRM_IRU3013	Rev. 0.0
			APPROVED MACRO	DESIGNED PING	DRAWN JOYCE	CUSTOMER NAME EPoX	JOB No. -	Sheet 20 of 21		









			EPoX COMPUTER CO., LTD	SCALE NONE	DRAWING DATE 2002-07-26	DRAWING TITLE D815E	Size A3	Description LAN1_82562EM	Rev. 0.0
			APPROVED MACRO	DESIGNED PING	DRAWN JOYCE	CUSTOMER NAME EPoX	JOB No. -	Sheet 21 of 21	

Exhibit A

M815A / ODM

Industrial ATX Board for Pentium® !!! Processor

Preliminary Specifications:

Processor: (Not Included)
- Intel® Celeron™ Processor with PPGA/FCPGA socket 370
  packing: operating at 433 ~ 1.1GHz
- Intel® Pentium® !!! /Coppermine™ Processor with FC-PGA
  or FC-PGAII w/HIS.
  socket 370 packing: operating at 500MHz ~ 1.1GHz

Core Logic:
- Intel® 82815E

BIOS:
- Award BIOS

FSB:
- 100 / 133 MHz

Memory:
- Two 168-pins DIMM sockets, support up to 512MB

IDE:
- PIO Mode, DMA Mode and one channel for up to 2IDE Devices

LAN Controller:
- Onboard Intel 82562 EM
  10/100 Base-TX Ethernet
- Onboard one RJ-45 connector

VGA function:
On-die Intel 815E chip integrated with 2D/3D graphic controller

USB:
- 2 x USB ports (Upper and lower, on Rear I/O)

Expansion Slots:
- 1 x 4XAGP slot

Golden finger :
- PCI signals according customer's assignment

Power connector :
- Power assignement provided by customer.

Environments:
- Operation temperature: 0°C to 60°C,
- Storage temperature: -20°C to 80°C,
- Relative humidity: 10% to 90% (Non-Condensing)

Dimensions (D x W):
- 190 mm x 187.01 mm
  Height according to 3D's drawing provided by customer.

Specification is subject to change accordiing to design concern
Or customer's requirement.

Remarks :

1. Power is not existed with VCC5 SBY, VDIMM3, -12V & -5V.

2. PCI1 is not standard and not compatible.
   PCI1: B1, B2, B3,B4, A1, A2, A3, A4 will be VCC12
   PCI1: B5, B6, B7, B8, B9 will be respectively RST, BCLK, SDOUT, SDIN0, SYNC used for the AC97.
   PCI1: B10, B11, B12 will be respectively GPIO25, GPIO27, GPIO28.
   GAELCO will provide their PCI card for EPoX's validation.

3.JTAG of Pentium III connector is necessary.

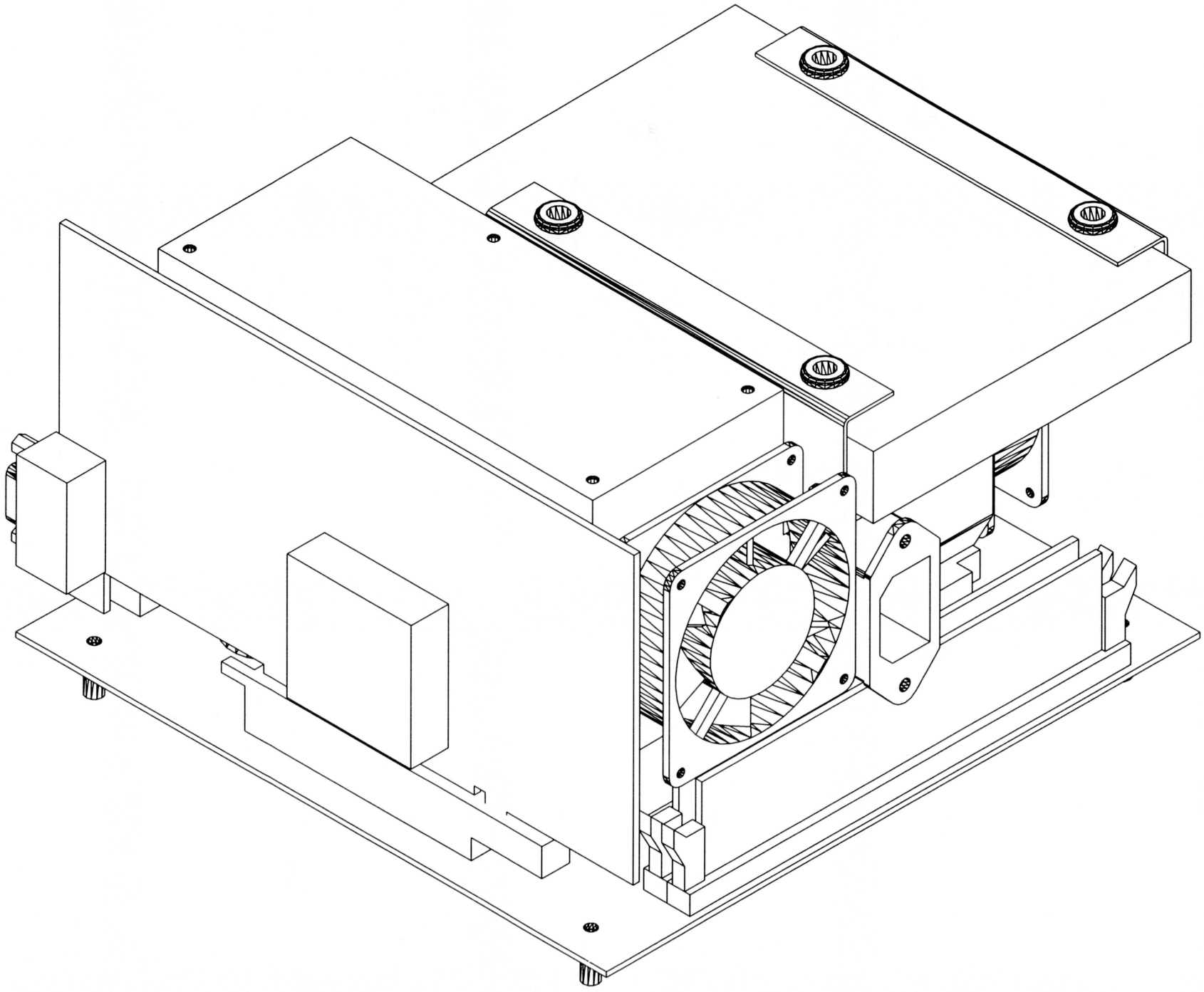
4. Operating system like Linux (Kernel 2.4.16) & Windows Embedded (Windows XP Kernel) will be modified by GAELCO and GAELCO also provide the finished OS for EPoX to test.

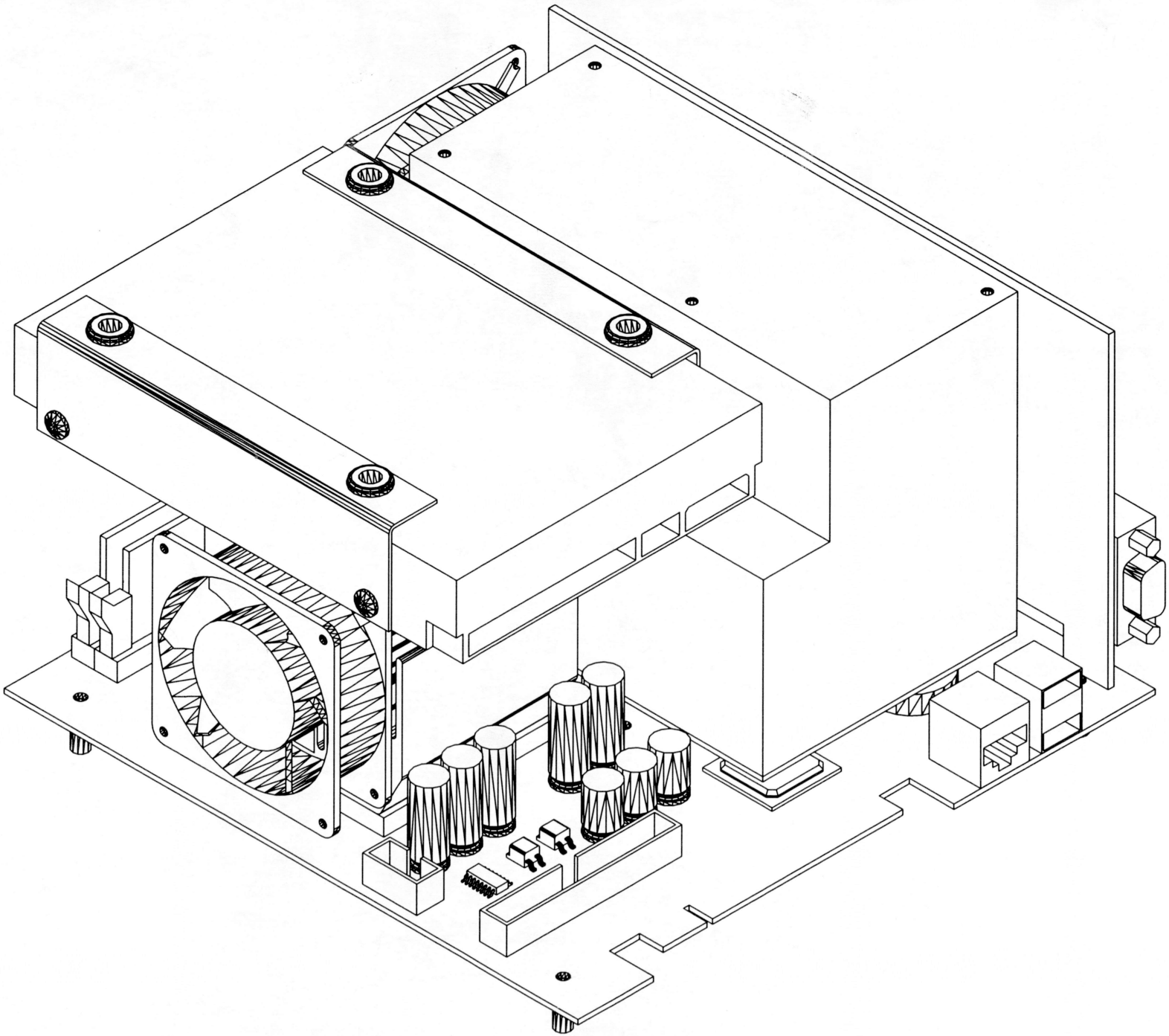
5. GAELCO will provide test program for EPoX to validate the ODM baord

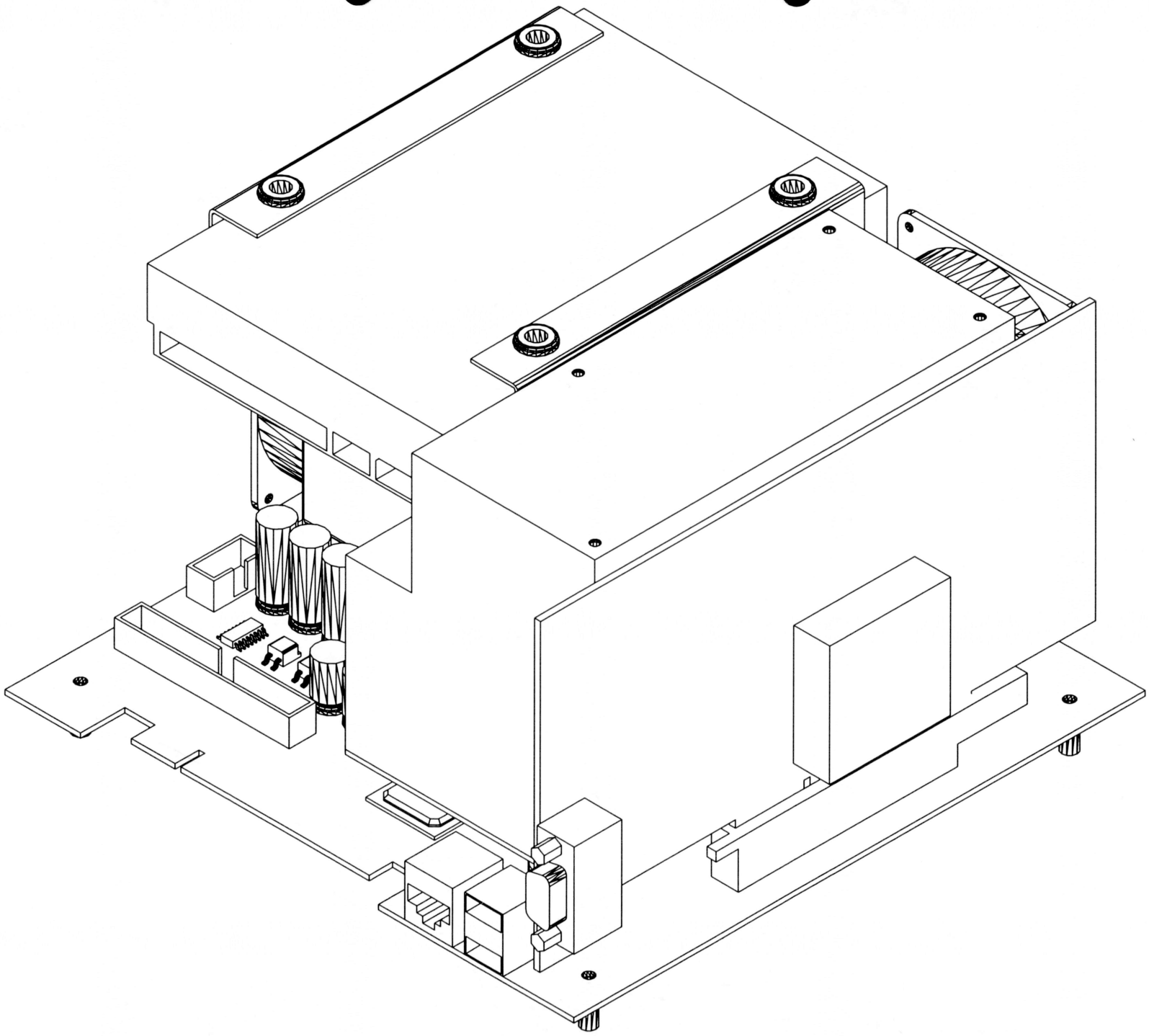
6. EPoX can modify the BIOS configuration in case it's required for any unsupported hardware changes. The NRE charge is US$ 4000.

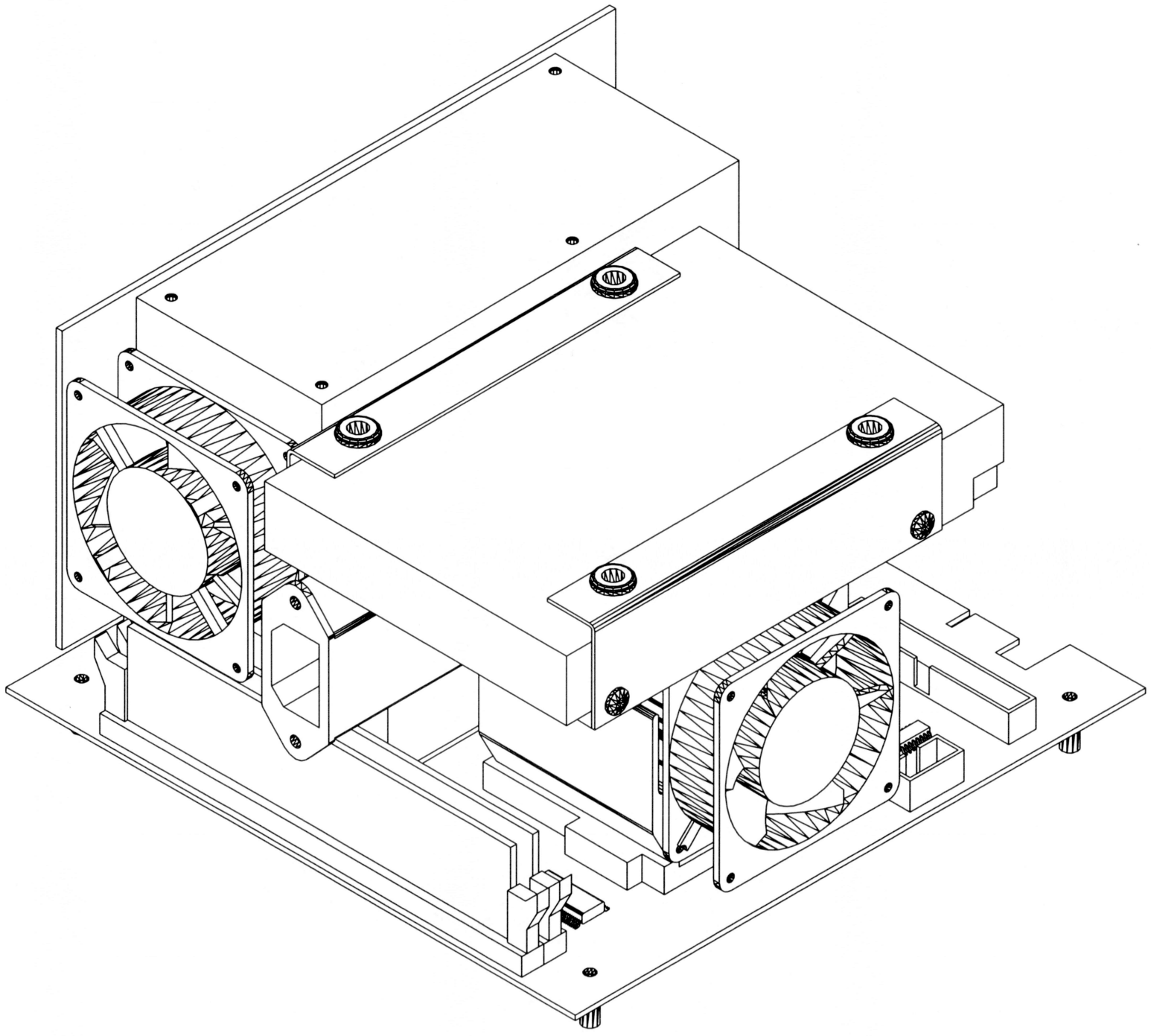
7. Only K/B is needed and will be connected through USB port.

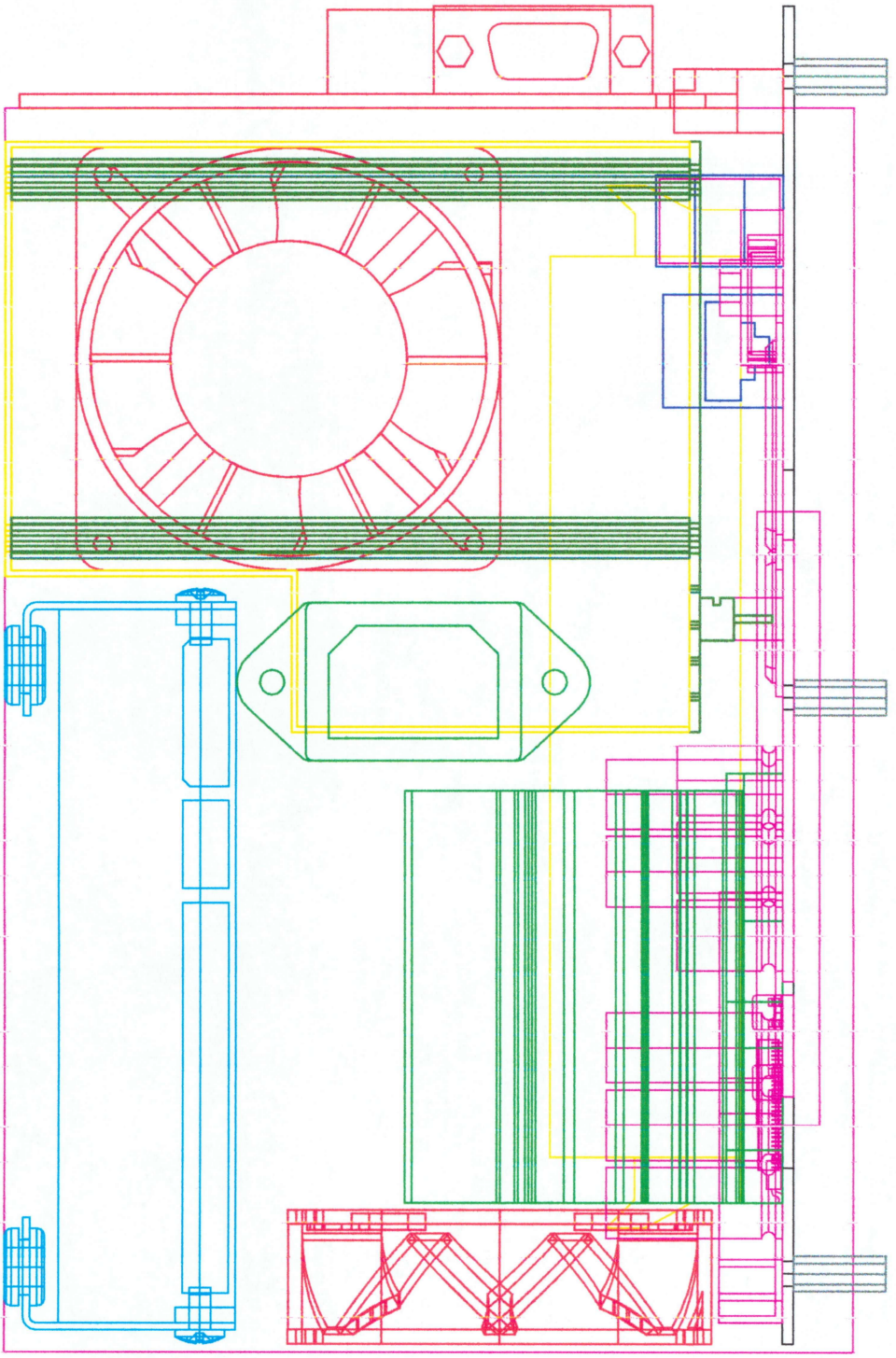
8. Customer will not need any block mechanism for the ODM board.

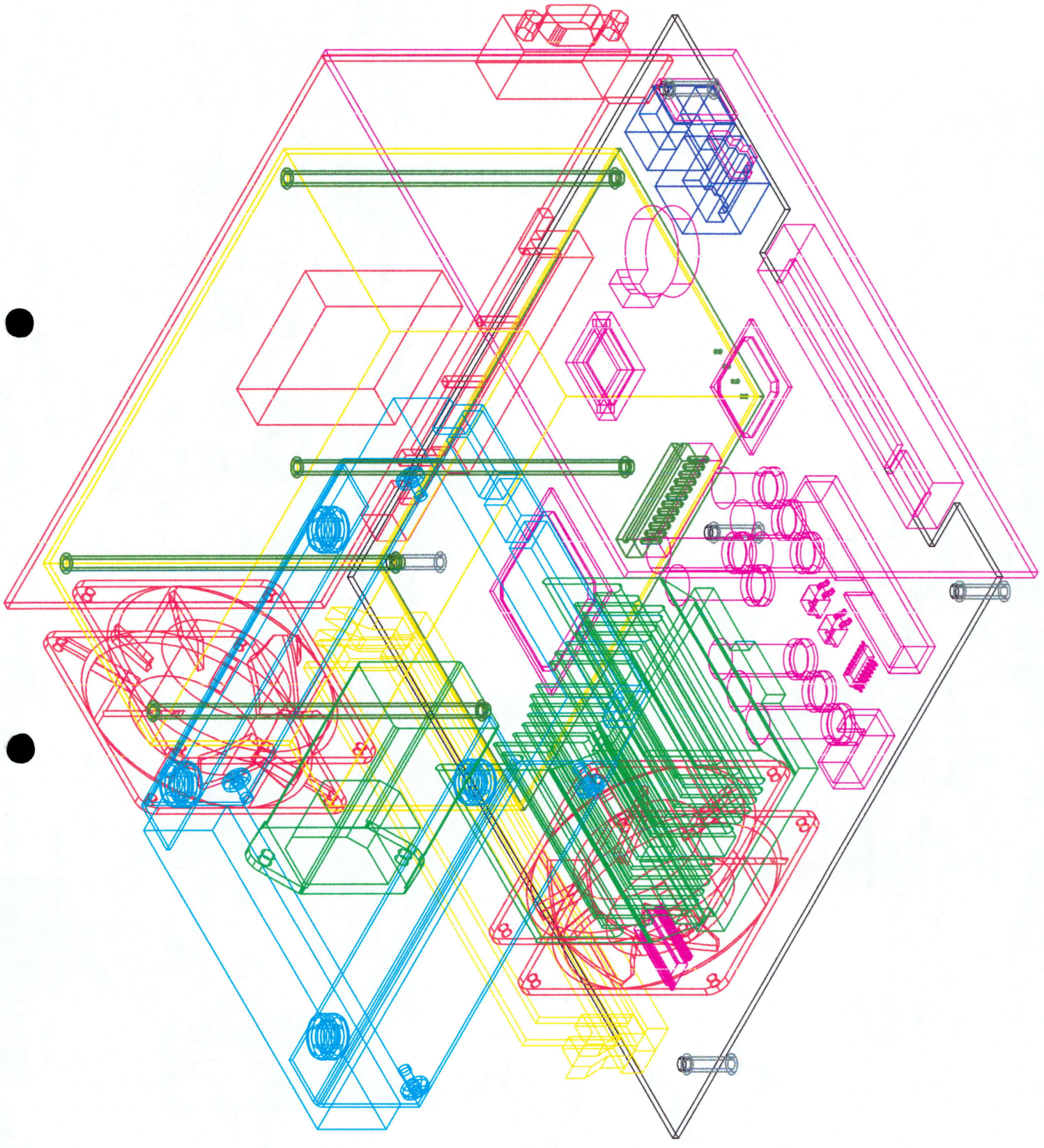


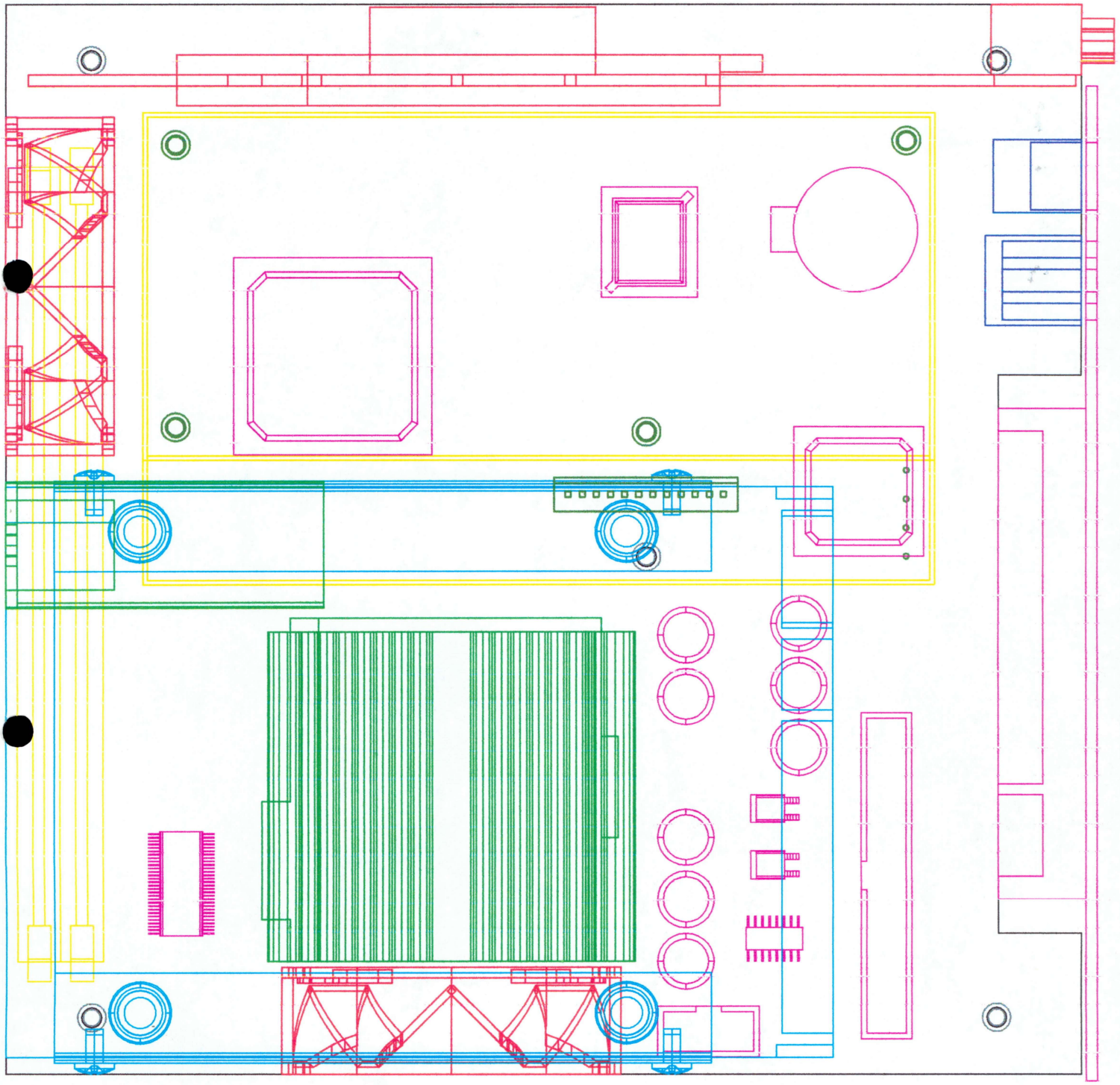


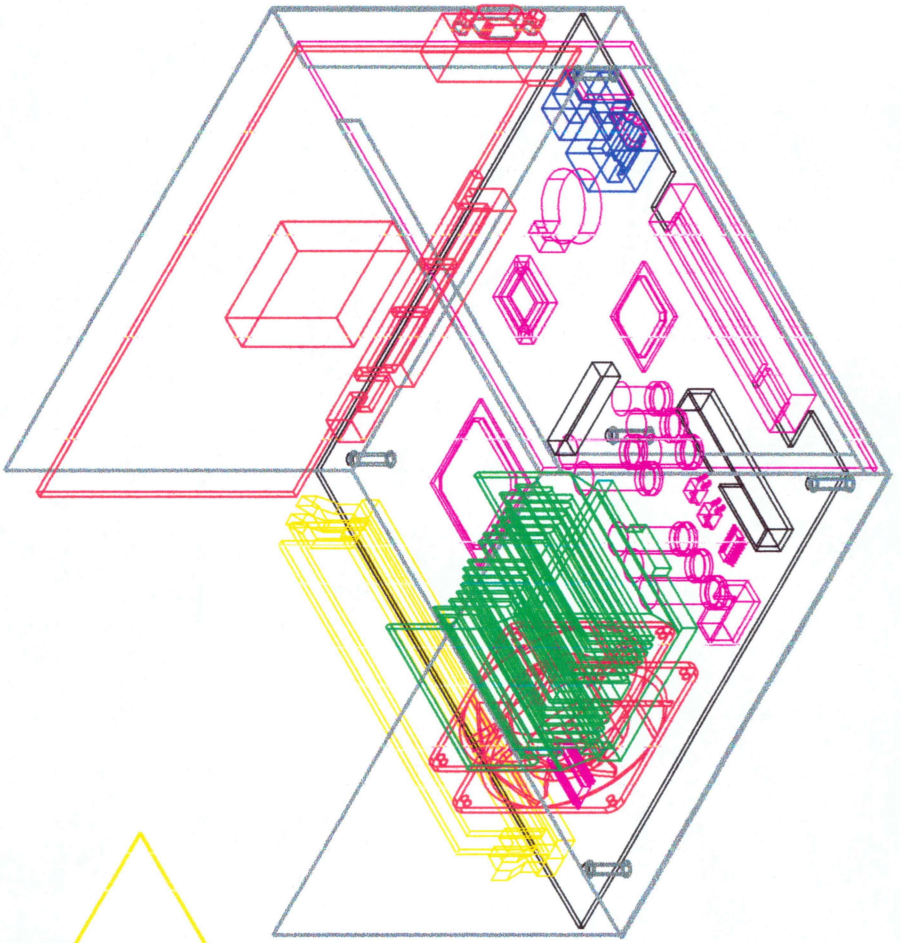


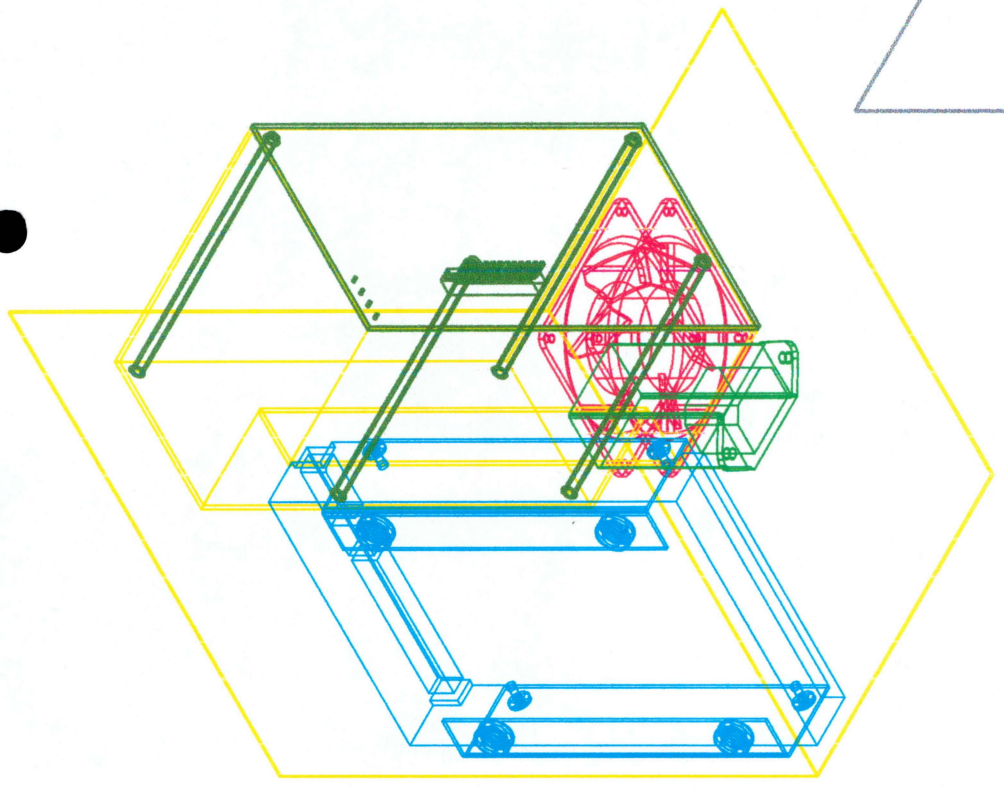


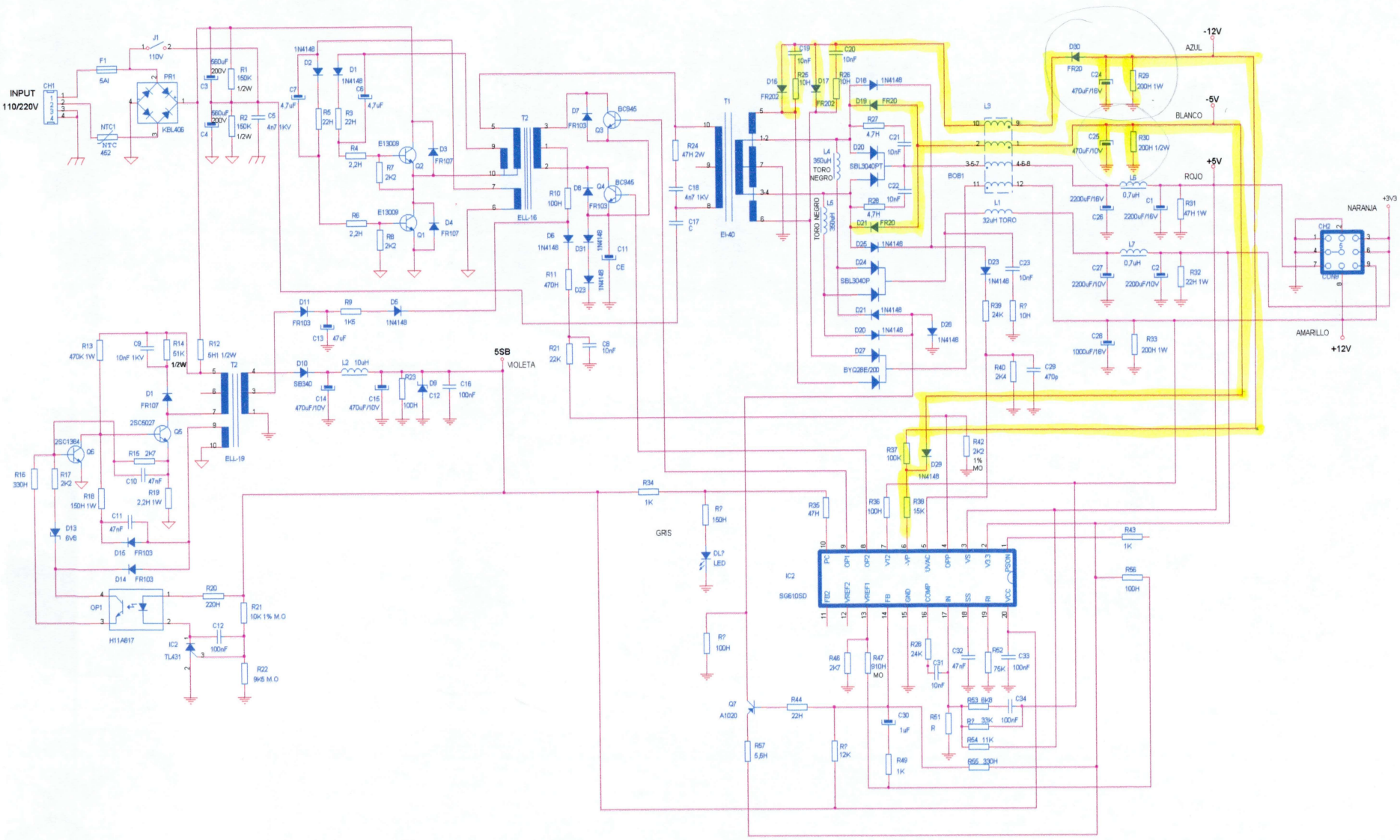


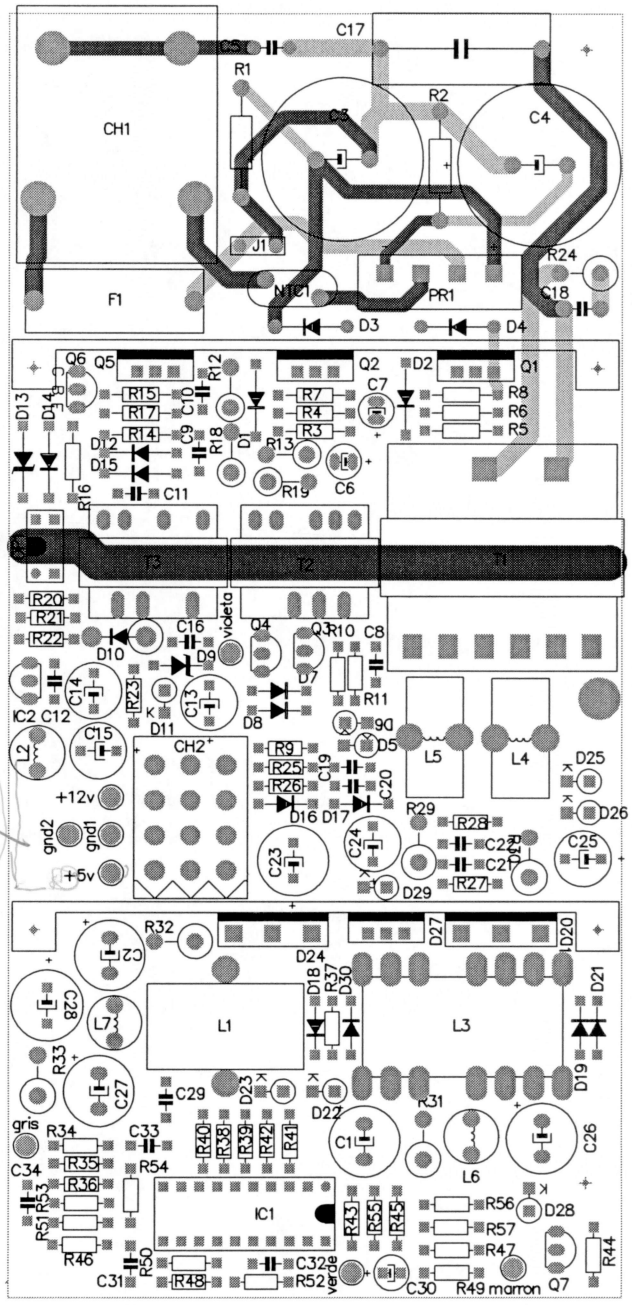






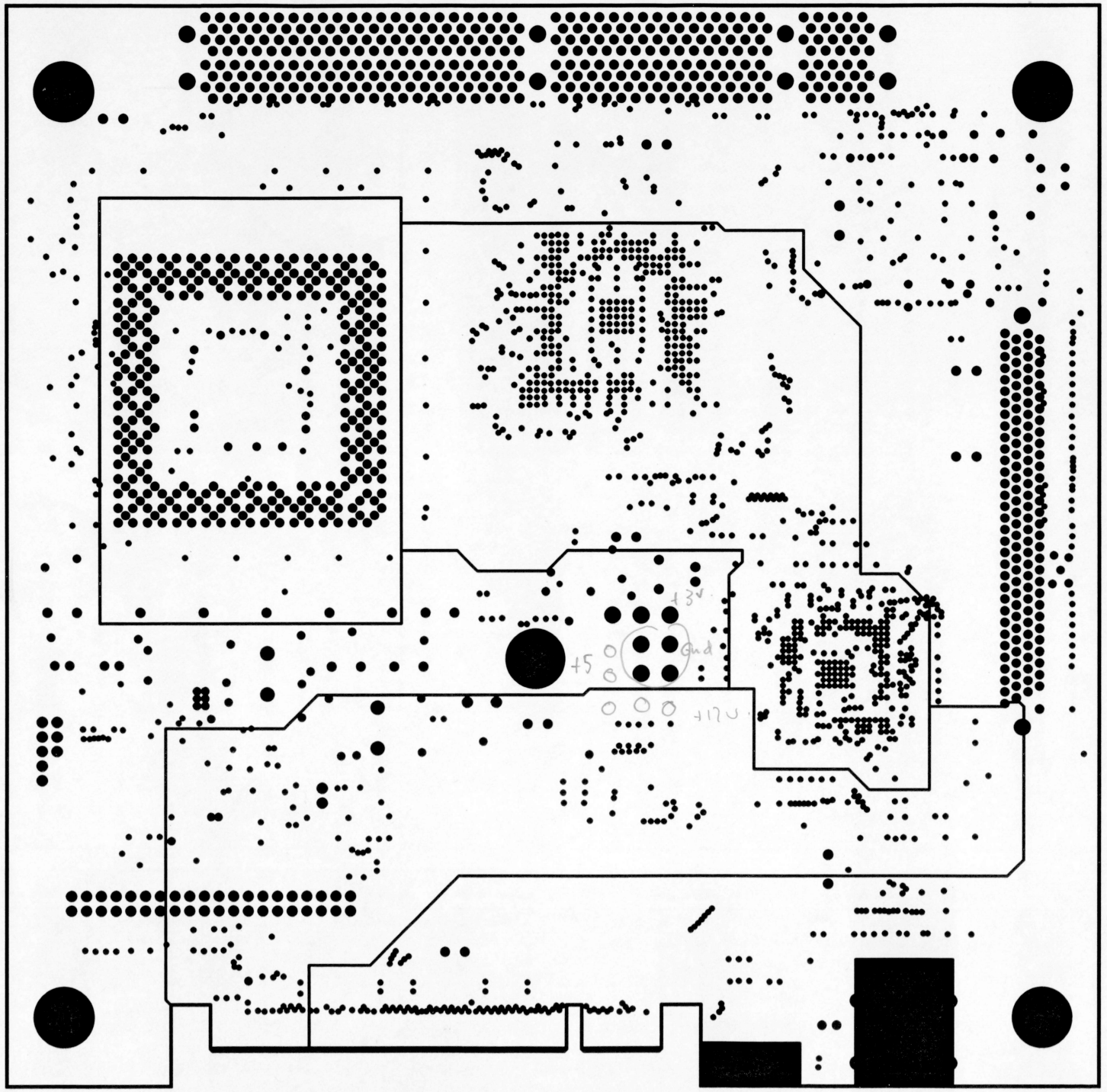


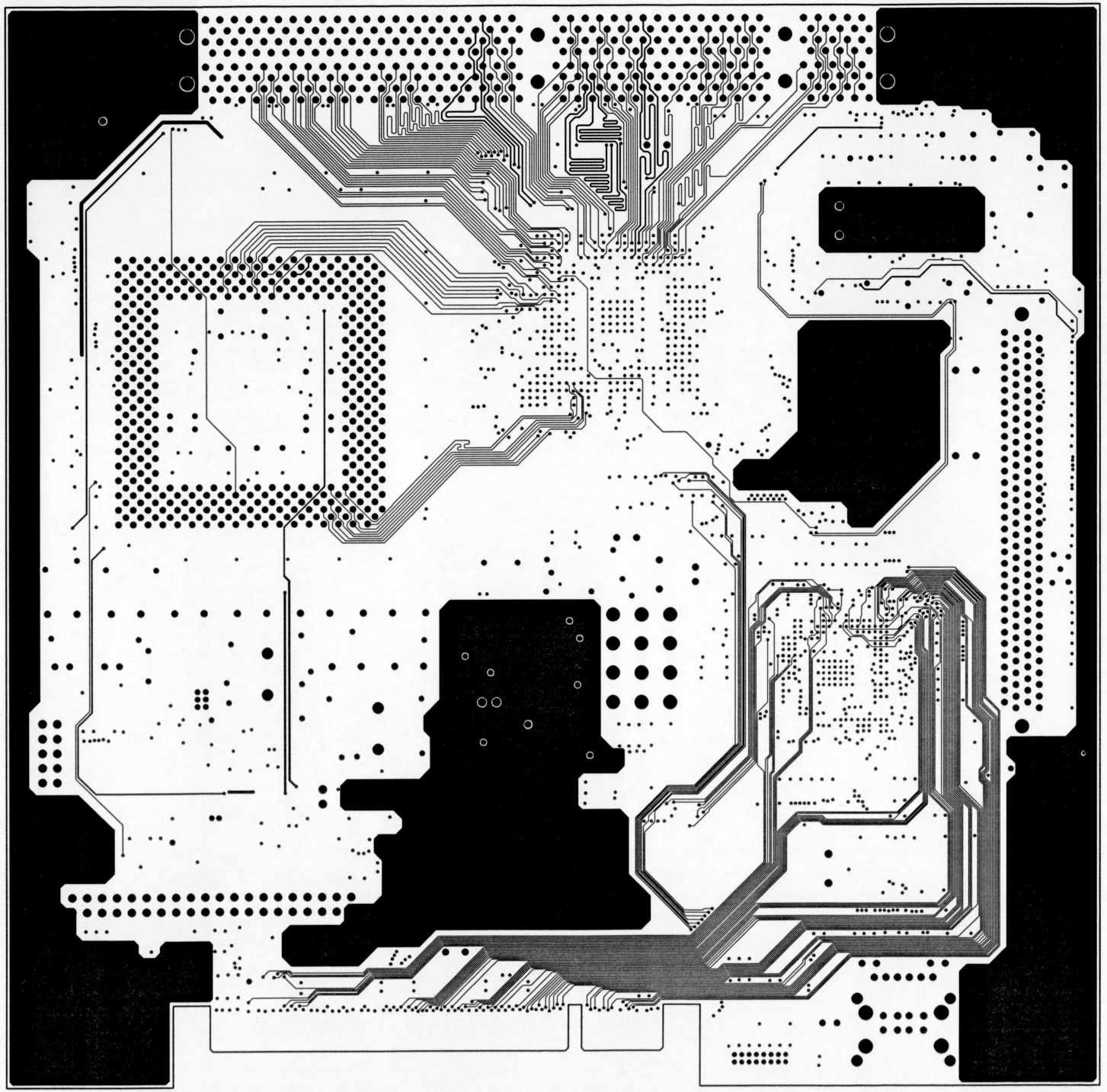

INPUT
110/220V
CH1
J1
110V
F1
5AI
PR1
KBL406
NTC1
NTC 4S2
C3
560uF 200V
C4
560uF 200V
R1 150K 1/2W
R2 150K 1/2W
C5 4n7 1KV
C7 4.7uF
1N4148
D2
D1 1N4148
C6 4,7uF
R5 22H
R3 22H
R4 2,2H
E13009
Q2
D3 FR107
R7 2K2
R6 2,2H
E13009
Q1
D4 FR107
R8 2K2
T2
ELL-16
D7 FR103
BC946
Q3
D6 1N4148
R10 100H
Q4 BC945
FR103
D31 1N4148
R11 470H
D23 1N4148
C11 CE
T1
EI-40
R24 47H 2W
C18 4n7 1KV
C17 C
C19 10nF
C20 10nF
R25 10H
R26 10H
D16 FR202
D17 FR202
D18 1N4148
D19 FR20
R27 4,7H
D20 SBL3040PT
C21 10nF
C22 10nF
R28 4,7H
D21 FR20
L4 350uH TORO NEGRO
L5 350uH TORO NEGRO
D25 1N4148
D24 SBL3040P
D21 1N4148
D20 1N4148
D27 BYQ28E/200
D26 1N4148
D23 1N4148
C23 10nF
R39 24K
R? 10H
R40 2K4
C29 470p
D11 FR103
R9 1K5
D5 1N4148
C13 47uF
R21 22K
C8 10nF
5SB
VIOLETA
R13 470K 1W
C9 10nF 1KV
R14 51K 1/2W
R12 5H1 1/2W
T2
ELL-19
D1 FR107
2SC5027
Q5
2SC1364
Q6
R15 2K7
C10 47nF
R16 330H
R17 2K2
R18 150H 1W
R19 2,2H 1W
C11 47nF
D13 6V8
D15 FR103
D14 FR103
OP1
H11A817
R20 220H
R21 10K 1% M.O
C12 100nF
IC2
TL431
R22 9K8 M.O
D10 FR20
C24 470uF/16V
R29 200H 1W
C25 470uF/10V
R30 200H 1/2W
L6 0,7uH
C1 2200uF/16V
C26 2200uF/16V
R31 47H 1W
L7 0,7uH
C27 2200uF/10V
C2 2200uF/10V
R32 22H 1W
C28 1000uF/16V
R33 200H 1W
L3
BOB1
L1 32uH TORO
-12V
AZUL
-5V
BLANCO
+5V
ROJO
+3V3
NARANJA
CH2
CONN
AMARILLO
+12V
R34 1K
GRIS
R? 150H
DL? LED
R37 100K
D29 1N4148
R42 2K2 1% MO
R35 47H
R36 100H
R39 15K
IC2
SG6105D
R43 1K
R56 100H
R? 100H
R46 2K7
R47 910H MO
R28 24K
C31 10nF
C32 47nF
R52 75K
C33 100nF
Q7 A1020
R44 22H
C30 1uF
R51 R
R63 6K8
R? 33K
C34 100nF
R54 11K
R55 330H
R57 6,8H
R? 12K
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Size A2
Document Number FUENTE PC
Rev JOSEP
Date: Tuesday, December 31, 2002
Sheet 1 of 1

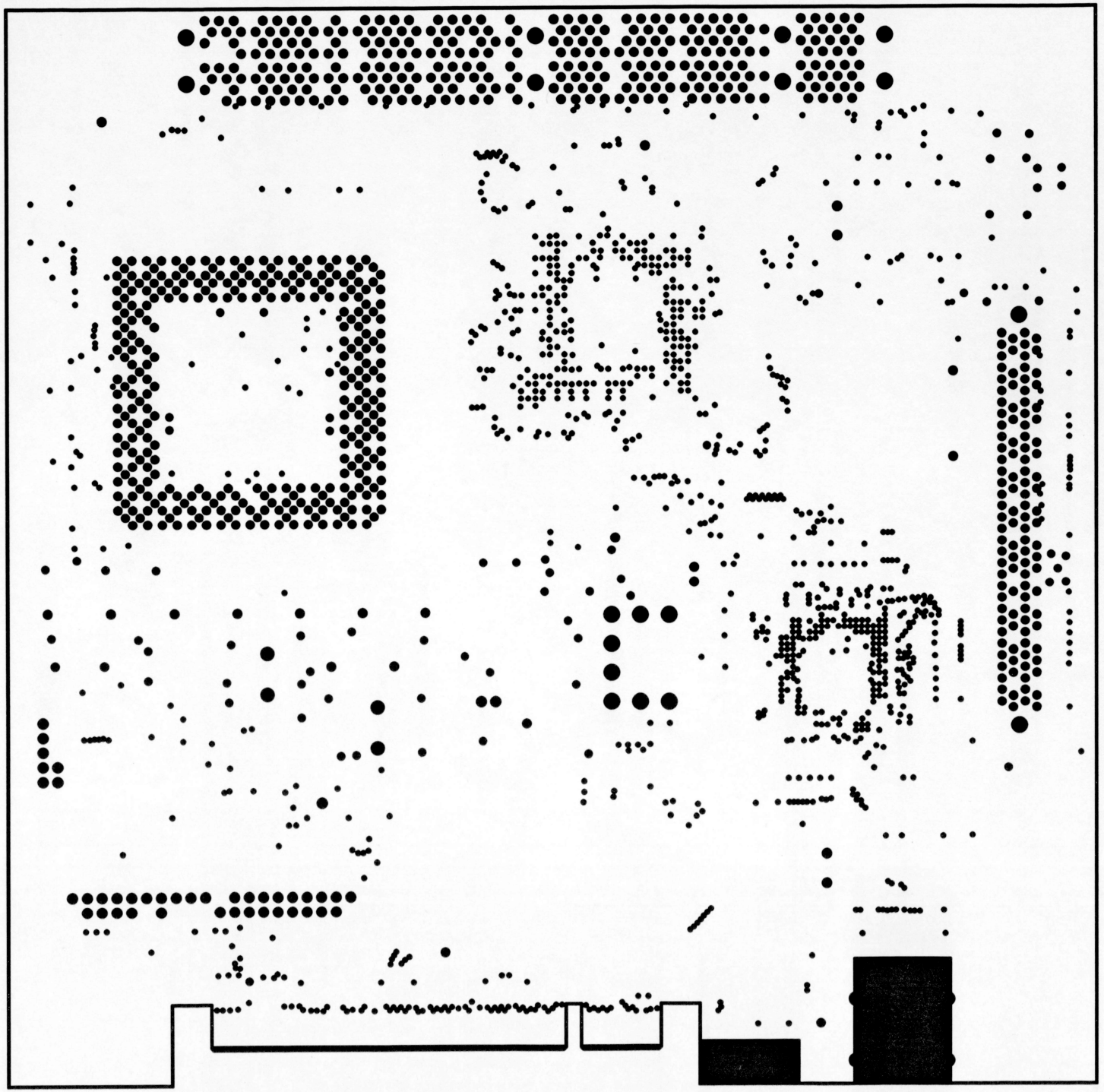


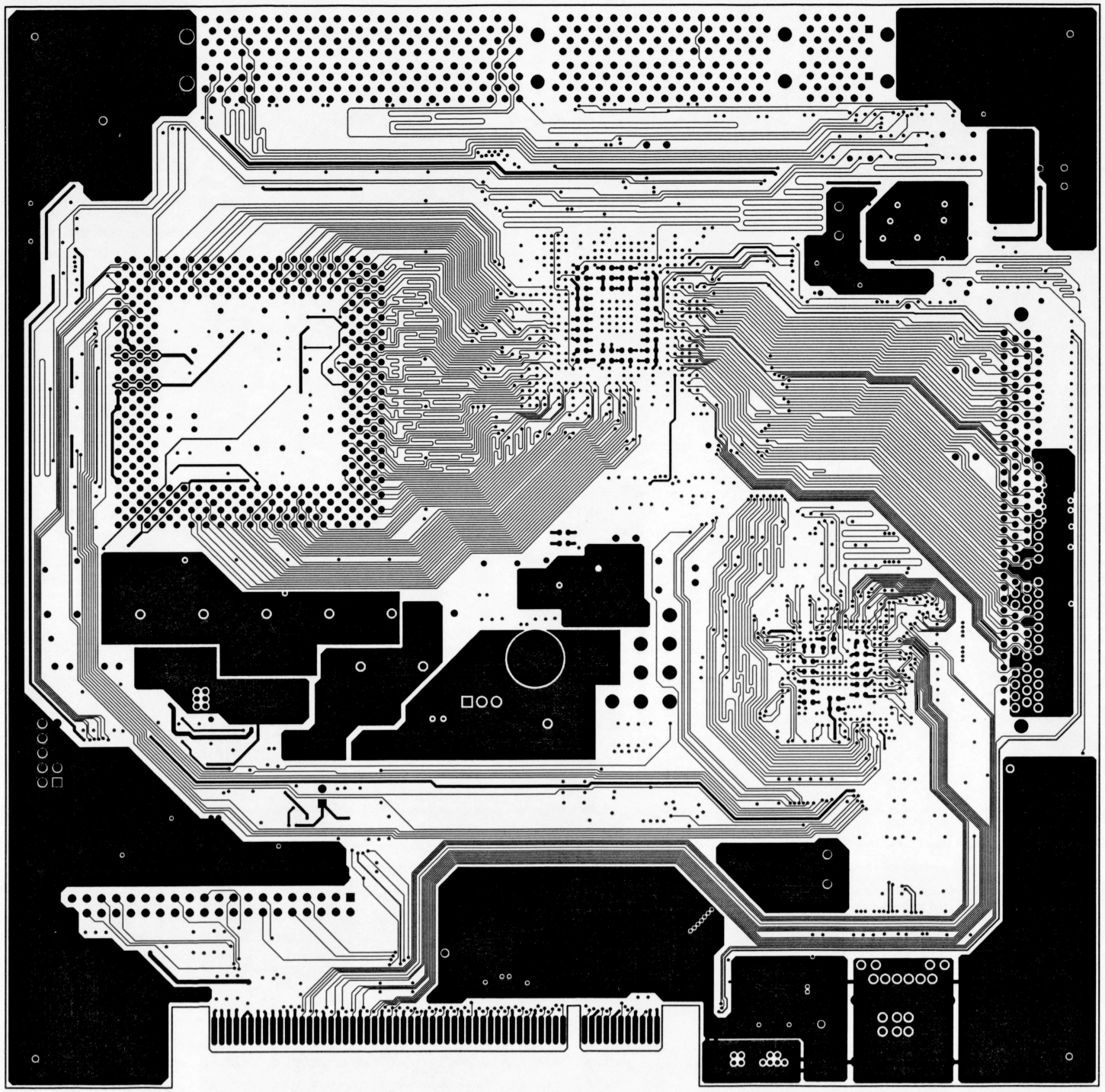
AERO43 160902

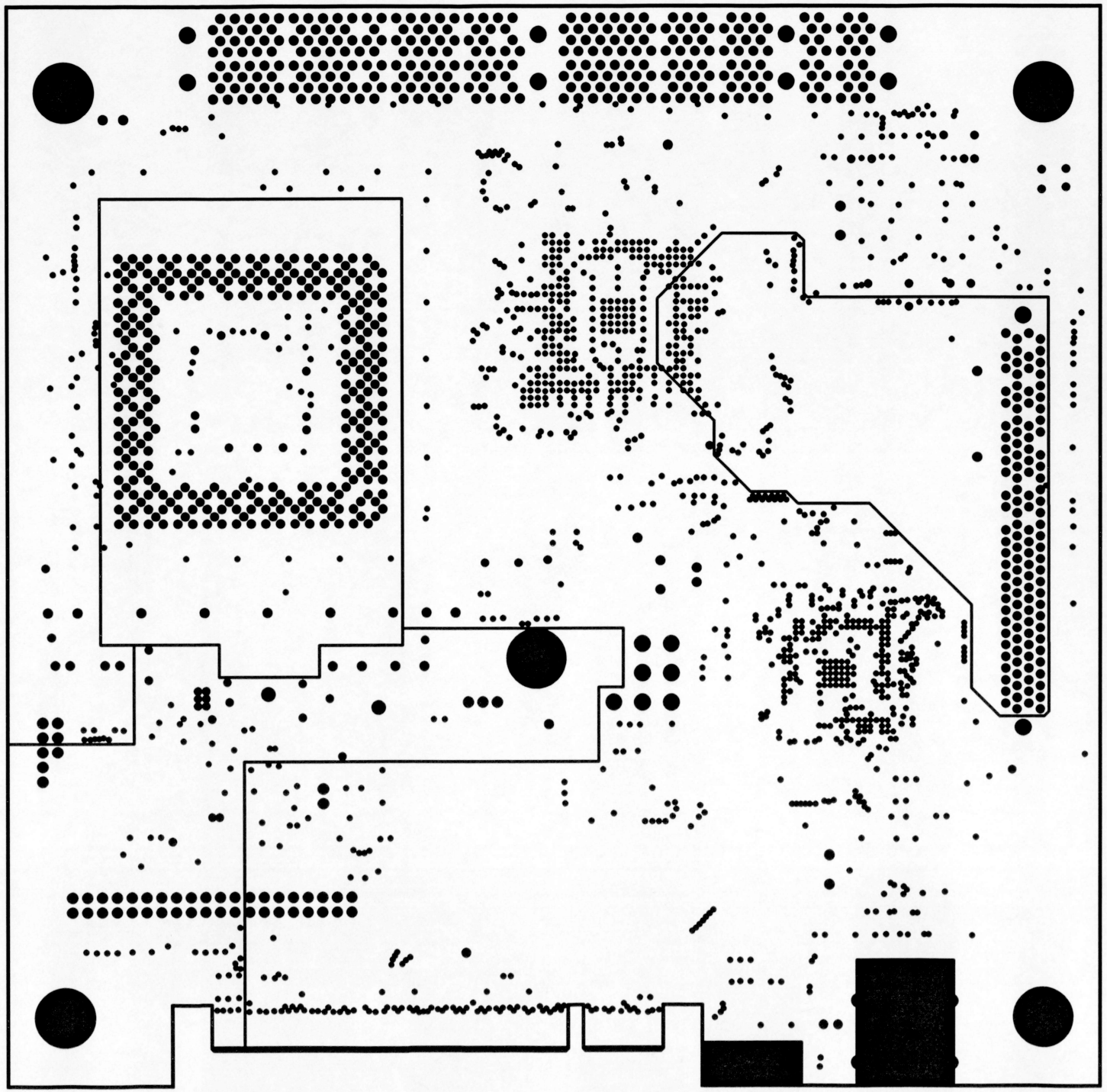
F. ALIMENTACION

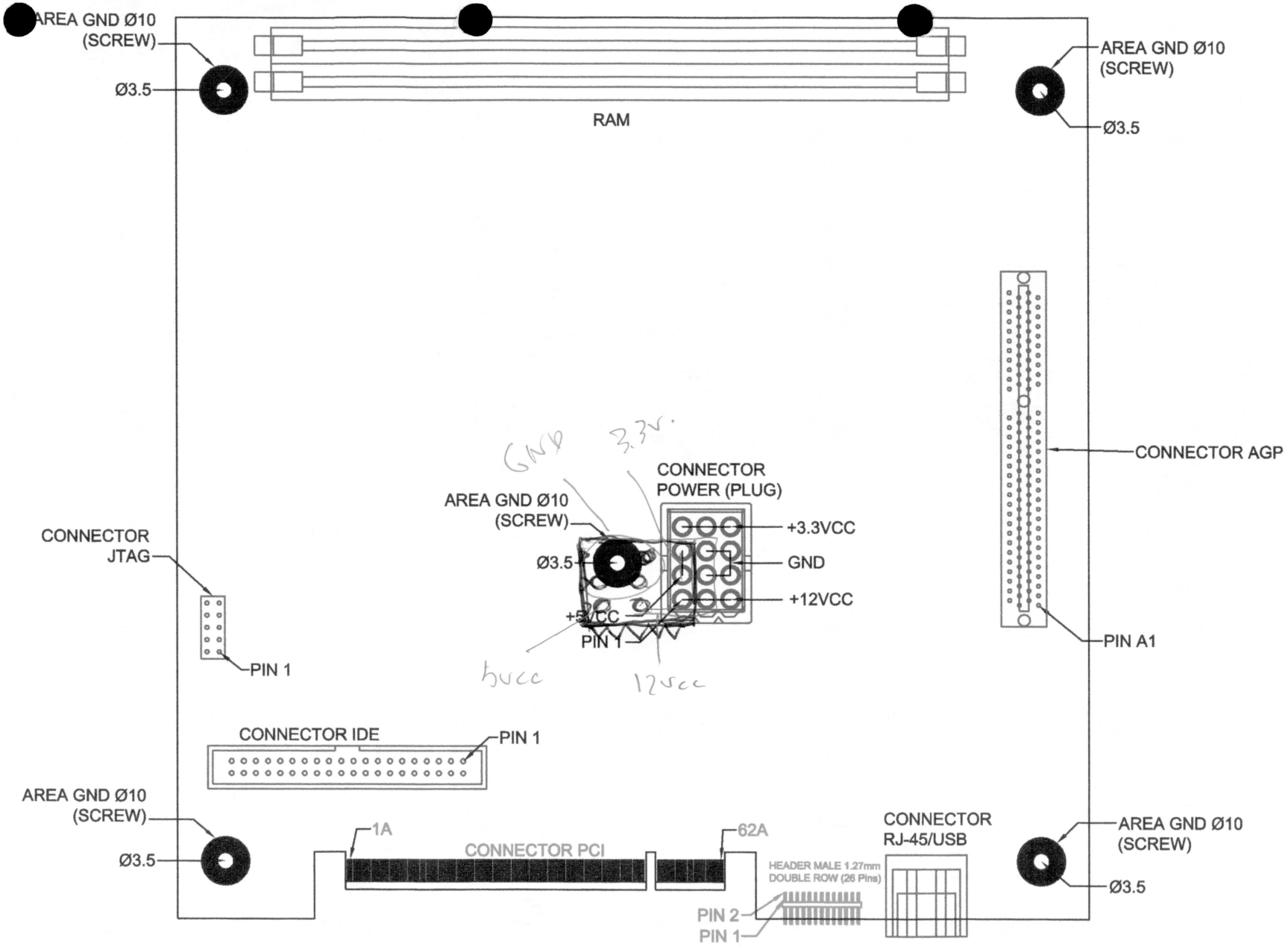

+3V
+5
Gnd
+12V











NOTA:
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS

Hardware specifications:

1- VCC5SBY voltage will be the same as VCC5. All SBY voltages will no exist. VDIMM3_3 voltage will be the same as VCC3.

2- VCC12- and VCC5M will no exist.

3- Power supply will be specific for this board and will be made by GAELCO.

4- We will only have PCI1, and it will be special (not standard and not compatible). It will include different pin configuration(see point 5 and 6). The PCI1 plug will be a card plug gold covered. The female for this connector will be placed in the frontal designed by GAELCO. (this means that the male/female will be in the inverse order compared with a common PC, where the female is placed in the mainboard). See schematics.

5-The following PCI1 pins will have the function of VCC12:
B1,B2,B3,B4,A1,A2,A3,A4.

6- The pins of PCI1: B6,B5,B7,B8,B9 will be respectively:
RST,BCLK,SDOUT,SDIN0,SYNC (to be used for the AC97), and pins B10,B11,B12 will be GPIO25,GPIO27,GPIO28 respectively.

7- LAN support will be adapted through a RJ45 connector and a Intel 82562EM chip.

8- Only two USB ports will be used: Upper and Lower.

9- W83627HF will be removed, because we don't need its ports and its floppy support.

10-We will include a JTAG connector for the PentiumIII to emulate the process

11- The mainboard power connector will be MOLEX model Order No.: 03-09-2121 and its pins will be MOLEX Part No.: 02-09-2134

12- We will only use primary IDE port, it the schemes is shown its place and orientation.

13- Microprocessor must be PentiumIII up to 1.2GHz or Celeron up to 1.2GHz. Both using socket 370

14- SDRAM sockets will be 168pins DIMM1 and DIMM2. We will use AGP 4X.

15- The mainboard must have a standard CPU fan connector (3 pins)

16- There will be no CMOS, its parameters will be inside FWH(BIOS)

17- We will not use W83628F, W83629D and XC9536XL chips, so we will not have any ISA bus.

18- The board will not have any EMIS filter, but its design will be optimized to minimize them.

19-We don't need AC'97 codec (it will be placed in the front board), we also don't need PRINTER PORT, GAME&MIDI, COM1, COM2, J5, J6.

20- The board does not need WDOG but we need a reset mini-switch and a checking chip that will notify when the 5VCC go below 4.68V (aprox.) (we cannot see this feature at the schemes). This chip must generate a reset when the voltage is low, and remove the reset if the voltage raises again. (Maybe this feature is included in IRU3013?)

21- We have added a new 26-pin VGA output connector (see attached scheme). This connector includes both Flat panel (digital) and CRT output. So the connector of your scheme 18/21 must be removed.

You can fix the pin distribution as you want in order to optimize the router of the main board. This connector must have the following pins:

-LTVDATA(0,11)
-LTVBLANK#
-LTVCLKOUT(0,1)
-TVVSYNC
-TVHSYNC
-LTVDA
-LTVCL
-VSYNC
-HSYNC
-RED
-GREEN
-BLUE
-AGND
-AGND

22- CNR SLOT is not necessary.

~~23- The board will include an output connector for the 815E built-in VGA.~~

24- RTC function of 82801 must be available an working, for this reason we need VCMOS voltage coming from a battery that we cannot see in your schemes. So this battery must be included

25- The placement of the CPU socket 370 can be fixed by your own in order to maintain standard spacing of the components (to avoid spacing problems with standard CPU cool radiators)

26- We think that 93C46 (U11 chip from scheme 21) is not necessary. Please, notify the reason to include it.

27- Regarding PCI gold finger: We are supposing that the A-pins are in the component side, and B-pins in the solder side. Please, notify if this is right.

Consideraciones del desarrollo

1° La tensión de VCC5SBY, será la misma que la VCC5. y todas las tensiones SBY no existirán, la tensión VDIMM3_3 será VCC3.
2° No tenedremos tension de VCC12- ni de VCC5M.
3° Los consumos serán VCC5_7,5A, VCC3_7,5A, VCC12_7,5A. y la tensión 110/220Vac
4° Los pines del PCI1 B1,B2,B3,A1,A2,A3,A4, pasarán a tener la función de VCC12.
5° Los pines del PCI1 B4,B14,A9,A11,A14 serán RST,BCLK,SDOUT,SDIN0,SYNC del AC97 respectivamente, y los B9,B10,B11 serán GPIO25,GPIO27,GPIO28, libres.
6° Adaptaremos la LAN para ETHERNET 10/100, con un conector J45 con el nuevo chip de INTEL.
7° Tendremos dos USB ports el Upper y el Lower.
8° Tendremos una adaptacion del bus PCI de carta en el circuito principal y el conector en el panel frontal.
9° Si se puede suprimir el W83627HF el KEYBOERD entrará por un USB, si no el conector PS2 MOUSE y el KEYBOARD estaran en el circuito camuflados. No hace falta que se protejan contra EMIS.
10° Pondremos un conector JTAG del PENTIUM III para emular el procesador.
11° El conector de la fuente irá transversal y tanto la hembra como el macho iran soldados a sus circuitos.
12°. Del circuito de la fuente saldran los cables para alimentar el disco duro, con el conector estandar (IDE primario).
13° Solo tendremos el bus IDE_PRIMARIO orientado y situado en su lugar
14° El pentium III debe ser FC-PGAII w/IHS o bien el FC-PGA.
15° Los zocalos de SDRAM serán DIMM1 y DIMM2 de 168 PIN y conservaremos el AGPX4.
16° El ventilador del procesador deberia ir lateral, expulsando aire al exterior con lo cual el radiador sera diferente y el zocalo no debe ser necesariamente de inserción zero.
17° El ventilador de la fuente expulsará aire al exterior
18° Debemos prescindir de la CMOS, W83628F, W83629D, XC9536XL.
19° Los parametros de la CMOS estaran definidos en el FWH (BIOS)
20° Situar el conector de alimentación y el selector de 220/110 VAC en su sitio.
21° La fuente llevará un filtro de conducidas hasta 30Mhz, las frecuencias superiores las filtraremos al traspasar el chasis con otro filtro.
22° El panel frontal lo realizará GAELCO.
23° EL Codec'97 irá en la placa frontal junto con los amplificadores.
24° No necesitamos AC'97Codec, PRINTER PORT, GAME & MIDI, COM1, COM2, J5, J6.
25° La placa no necesita WDOG pero si un micro pulsador de RESET.
26° El conector de SVGA saldrá directamente de la tarjeta aceleradora.
27° El chip MCH no hace falta que lleve la versión para VGA.
28° El sistema operativo será un LINUX modificado por GAELCO para correr en tiempo real.

13/03/2002

Hardware specifications:

1- VCC5SBY voltage will be the same as VCC5. All SBY voltages will no exist. VDIMM3_3 voltage will be the same as VCC3.

2- VCC12- and VCC5M will no exist.

3- Power supply will be specific for this board and will be made by GAELCO.

4- We will only have PCI1, and it will be special (not standard and not compatible). It will include different pin configuration(see point 5 and 6). The PCI1 plug will be a card plug gold covered. The female for this connector will be placed in the frontal designed by GAELCO. (this means that the male/female will be in the inverse order compared with a common PC, where the female is placed in the mainboard). See schematics.

5-The following PCI1 pins will have the function of VCC12: B1,B2,B3,B4,A1,A2,A3,A4.

6- The pins of PCI1: B6,B5,B7,B8,B9 will be respectively: RST,BCLK,SDOUT,SDIN0,SYNC (to be used for the AC97), and pins B10,B11,B12 will be GPIO25,GPIO27,GPIO28 respectively.

7- LAN support will be adapted through a RJ45 connector and a Intel 82562EM chip.

8- Only two USB ports will be used: Upper and Lower.

9- W83627HF will be removed, because we don't need its ports and its floppy support.

10-We will include a JTAG connector for the PentiumIII to emulate the process

11- Power connector between power supply board (male) and main board (female) must be defined (both connectors must be to mount over PCB, not wires).

12- We will only use primary IDE port, it the schemes is shown its place and orientation.

13- PentiumIII must be FC-PGAII w/IHS or FC-PGA

14- SDRAM sockets will be 168pins DIMM1 and DIMM2. We will use AGP 4X.

15- We will use only the Pentium cool fan, that will go with a fixed 12VCC plug.

16- There will be no CMOS, its parameters will be inside FWH(BIOS)

17- We will not use W83628F, W83629D and XC9536XL chips, so we will not have any ISA bus.

18- The board will not have any EMIS filter, but its design will be optimized to minimize them.

19-We don't need AC'97 codec (it will be placed in the front board), we also don't need PRINTER PORT, GAME&MIDI, COM1, COM2, J5, J6.

20- The board does not need WDOG but we need a reset mini-switch and a checking chip that will notify when the 5VCC go below 4.68V (aprox.)

21- The MCH chip will have VGA function built-in

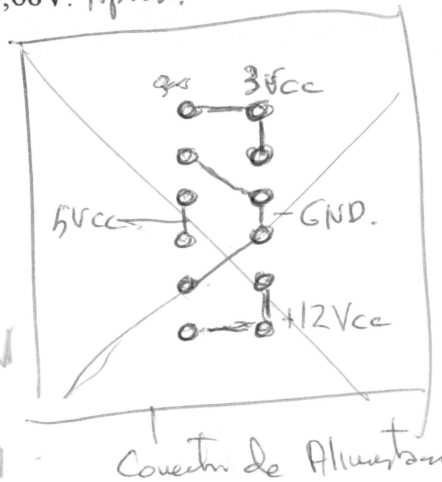
22- CNR SLOT is not necessary.

23- The board will include an output connector for the 815E built-in VGA.

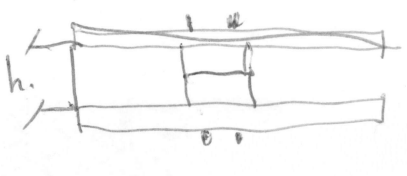
Consideraciones HARDWARE

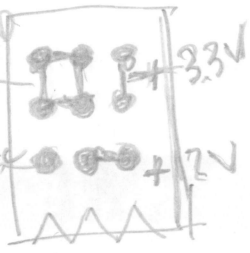
1° La tensión de VCC5SBY, será la misma que la VCC5. y todas las tensiones SBY no existirán, la tensión VDIMM3_3 será VCC3.
2° No tenedremos tension de VCC12- ni de VCC5M.
3° La fuente sera especial para esta placa y en principio la realizará GAELCO.
4° Solo tendremos el **PCI1**, y será especial (no estandar ni compatible), a parte de tener los pines diferentes (definidos en los apartados 4° y 5°) el conector **PCI1** sera de carta bañado en oro en el circuito principal, y en el panel frontal que realizará GAELCO, se pondrá el conector (ver graficos del sistema mecanico).
5° Los pines del **PCI1** B1, B2, B3, A1, A2, A3, A4, pasarán a tener la función de VCC12.
6° Los pines del **PCI1** ~~B4, B14, A9, A11, A14~~ serán RST, BCLK, SDOUT, SDIN0, SYNC del AC97 respectivamente, y los ~~B9, B10, B11~~ serán GPIO25, GPIO27, GPIO28.
7° Adaptaremos la LAN para ETHERNET 10/100, con un conector RJ45 y el chip de INTEL 82562EM.
8° Tendremos solo dos USB ports el Upper y el Lower.
9° Se suprimirá el W83627HF , puesto que no necesitamos ningun port ni el floppy disc.
10° Pondremos un conector JTAG del PENTIUM III para emular el procesador.
11° Debemos definir el tipo de conector de alimentacion para que sea el macho y la hembra para soldadura en PCB.
12° Solo tendremos el bus IDE_PRIMARIO orientado y situado en su lugar según graficos.
13° El pentium III debe ser FC-PGAII w/IHS o bien el FC-PGA.
14° Los conectores de SDRAM serán DIMM1 y DIMM2 de 168 PIN y conservaremos el AGPX4.
15° Solo habrá el ventilador del PENTIUM que ira con un conector a 12VCC fijo.
16° No habrá CMOS y los parametros estarán definidos en la FWH (BIOS).
17° Debemos prescindir de los chips, W83628F, W83629D, XC9536XL y por lo tanto no tendremos ningun bus ISA.
18° No tendra la placa ningun filtro especial para las EMIS, pero si que el diseño estará optimizado para minimizarlas.
19° No necesitamos AC'97Codec (irá en el frontal), ni tampoco el PRINTER PORT, GAME & MIDI, COM1, COM2, J5, J6.
20° La placa no necesita WDOG pero si un mini pulsador de RESET y un chip SUPERVISOR para cuando los 5VCC bajan por debajo de 4,68V. Aprox.
21° El chip MCH no hace falta que lleve la versión para VGA.
22° El CNR SLOT no es necesario.

28/05/2002



Conector de Alimentación





REFUNDIDO DE ESPECIFICACIONES

CAMBIOS A PARTIR DE LOS ESQUEMAS Rev 0.1 2002-09-26

1°- El conector de alimentación se ha reducido a 9 pins y se ha desplazado, ver posicionamiento en graficos. El fabricante y el modelo sigue siendo el mismo.

2°- El conector de video digital pasa a ser el modelo xxxxxx y tendra la distribución siguiente.

Pin 1a	RED	Pin 1b	GREEN
Pin 2a	BLUE	Pin 2b	VSYNC
Pin 3a	HSYNC	Pin 3b	GND
Pin 4a	GND	Pin 4b	LTVDATA0
Pin 5a	LTVDATA3	Pin 5b	LTVDATA2
Pin 6a	LTVDATA1	Pin 6b	LTVDATA4
Pin 7a	LTVDATA5	Pin 7b	LTVDATA6
Pin 8a	LTVDATA7	Pin 8b	LTVDATA8
Pin 9a	LTVDATA9	Pin 9b	LTVDATA10
Pin 10a	LTVDATA11	Pin 10b	LTVBLANK
Pin 11a	LTVCLKOUT0	Pin 11b	LTVCLKOUT1
Pin 12a	TVVSYNC	Pin 12b	TVHSYNC
Pin 13a	LTVDA	Pin 13b	LTVCL

3°- El conector JTAG del PROCESADOR no hace falta montarlo en las placas.

4°- La placa usará la CMOS del RTC, si se saca la bateria se cargarán los parametros estandar que estan almacenados en la BIOS.

5°- La BIOS después de inicializar el B0:D30:F0 (GPIO) y antes del B0:D30:F0, debemos ejecutar un modulo de BIOS para inicializar la circuiteria que tenemos en el GOLD_FINGER. El codigo binario lo suministrará GAELCO. Este modulo residirá en la BIOS.